

PROJECT NAME : Herschel 15 GPP53  
PCB NO :LA-H32AP

# Compal Confidential

## Schematic Document

AMD APU Picasso/Dali

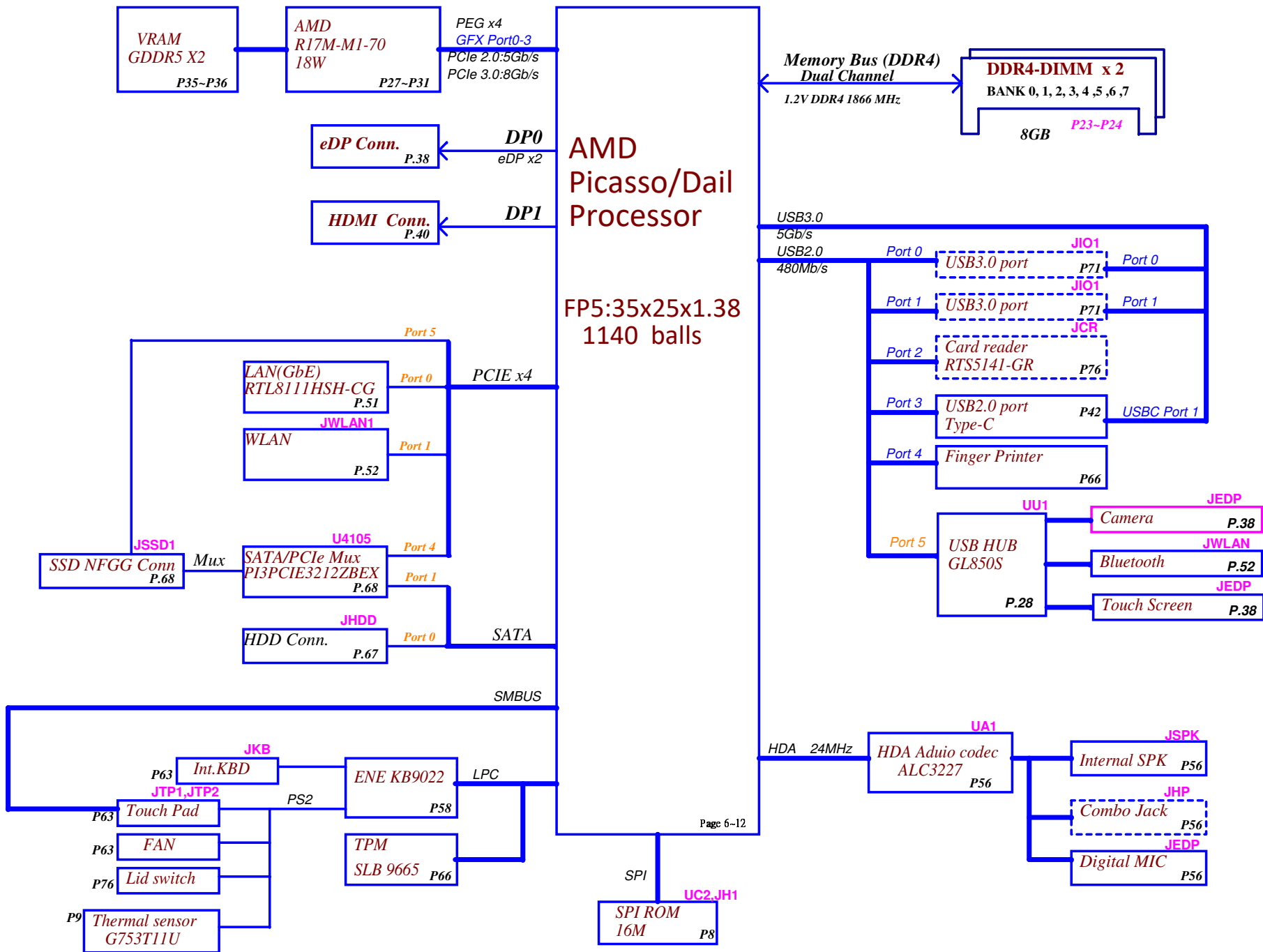
AMD GPU R17M-M1-70 (Radeon 530)

2019/11/01

Rev: 0.2



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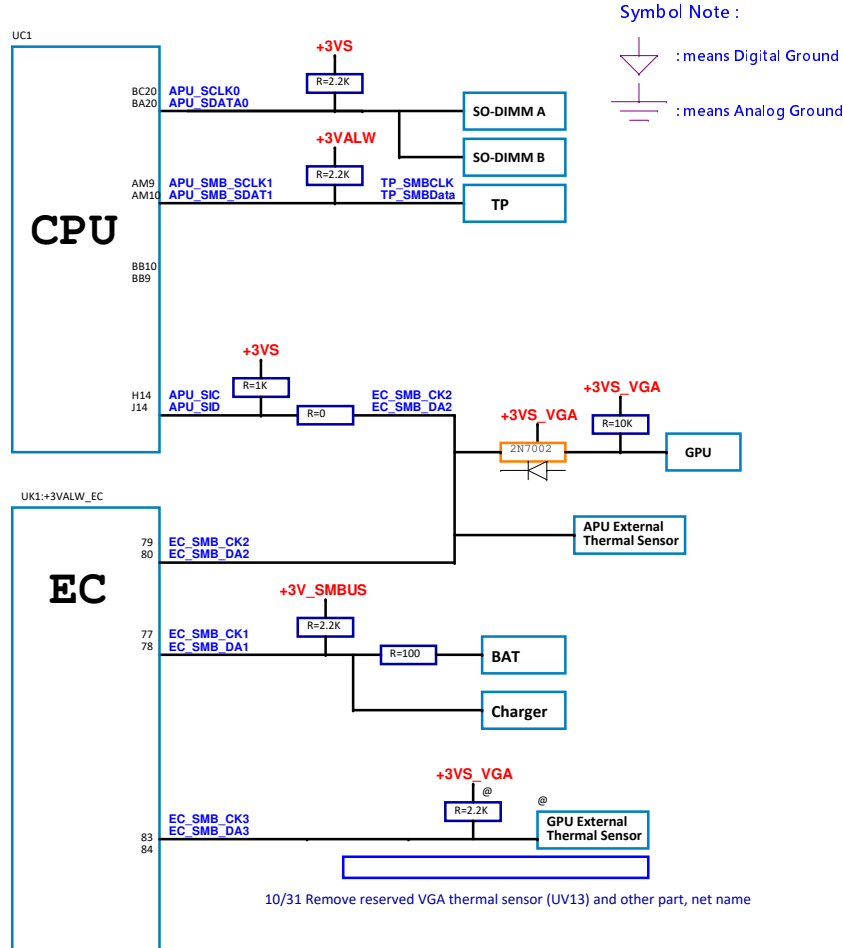
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Power rail	Control (EC)	Source (CPU)
+3V_LID	X	X
VIN	X	X
BATT+	X	X
+19VB	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	X	X
+1.2V_VDDQ	PG_+2.5V	PM_SLP_S5#/PM_SLP_S4#
+0.6VS_VTT	SUSP#	
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+APU_CORE		VR_ON
+APU_GFX		GFX_VR_OFF

@ is NO SMT part (empty)  
short@ : short pad , don't pop.  
@EMI@,@ESD@,@RF@ : Reserve , don't pop.  
RF@ : RF team request, must add.  
EMI@ : EMI team request, must add.  
ESD@ : ESD team request, must add.  
LVDS@ : Support LVDS panel.  
eDP@ : Support eDP panel.  
PX@ : GPU BOM config.

SOC SMBUS Address Table					
SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
APU_SCLK0 APU_SDAT0	+3VS	DIMMA	0x40	TBC	TBC
		DIMMB	0x41	TBC	TBC
APU_SMB_SCLK1 APU_SMB_SDAT1		Touch Pad	0X2C	TBC	TBC
APU_SIC APU_SID	+3VS	EC	0x1A	TBC	TBC
		Thermal Sensor	0x48	TBC	TBC
		LVDS		TBC	TBC

<USB Port>			
USB3.0 Port	DESTINATION	USB2.0 Port	DESTINATION
0 - 0	Type C	0 - 0	USB3 Type A
0 - 1	Type C	0 - 1	USB3 Type A
0 - 2	USB3 Type A	0 - 2	Card Reader
0 - 3	USB3 Type A	0 - 3	Type C
1 - 0 T1 only		1 - 0	FPR
		1 - 1	USB HUB



EC SMBUS Address Table					
EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SMBUS Port 1	+3VALW_EC	BAT	TBC	TBC	TBC
		CHGR	TBC	TBC	TBC
SMBUS Port 2	+3VS	APU Int sensor	0x4C	0x98	0x99
		DGPU Int sensor	0x41	0x82	0x83
		APU External Thermal Sensor	0x48	0x90	0x91

<PCI-E,SATA,CLK>			
	PCI-E	SATA	DESTINATION
	0		LAN
	1		WLAN
T1 only	2		X
T1 only	3		X
	4		PCI-E SSD
	5		PCI-E SSD
T2 SATA only	6	0	HDD
T2 SATA only	7	1	SSD or ODD
GFX		GPU	CLK0

45@	ROYALTY HDMI W/LOGO
Part Number	Description
R000000020M	HDMI W/Logo:R000000020M
R000000031M	

UC1	Athlon 300U_R1@ SAB000CFE20
UC1	Athlon 300U_R3@ SAB000CFE50
UC1	R3 3200U_R1@ SAB000CC540
UC1	R3 3200U_R3@ SAB000CC530
UC1	R5 3500U_R1@ SAB000CCR20
UC1	R5 3500U_R3@ SAB000CCR50
UC1	R7 3700U_R1@ SAB000C7640
UC1	R7 3700U_R3@ SAB000C7660

777	PCB
Part Number	Description
PCB PP05 LA-G07JP LS-G071P(G072P 02	

777	EMC for EE
X4E IL@	
X4EMW32L01	

U666	R70_R1@
R17M-M1-70 FCBGA	
SAB00009VH0	
S IC 216-0889018 A0 R17M-M1-70 FCBGA 0FH	

U666	R50_R1@
R17M-M2-50 FCBGA	
SAB00001W0	
S IC A32 216-0889004 A0 R17M-M2-50 BGA	

U666	R70_R3@
R17M-M1-70 FCBGA	
SAB00001V21	
S IC 216-0889018 A0 R17M-M1-70 GPU A321	

U666	R70_R1_FREE@
R17M-M1-70 FCBGA	
SAB00001V08	
S IC A32 216-0889018 A0 R17M-M1-70 FCBGA	

777	HY2_R1@
2G Hynix	
X7677232L01	

777	HY2_R3@
2G Hynix	
X7677232L07	

777	SAM2_R1@
2G Samsung	
X7677232L02	

777	SAM2_R3@
2G Samsung	
X7677232L08	

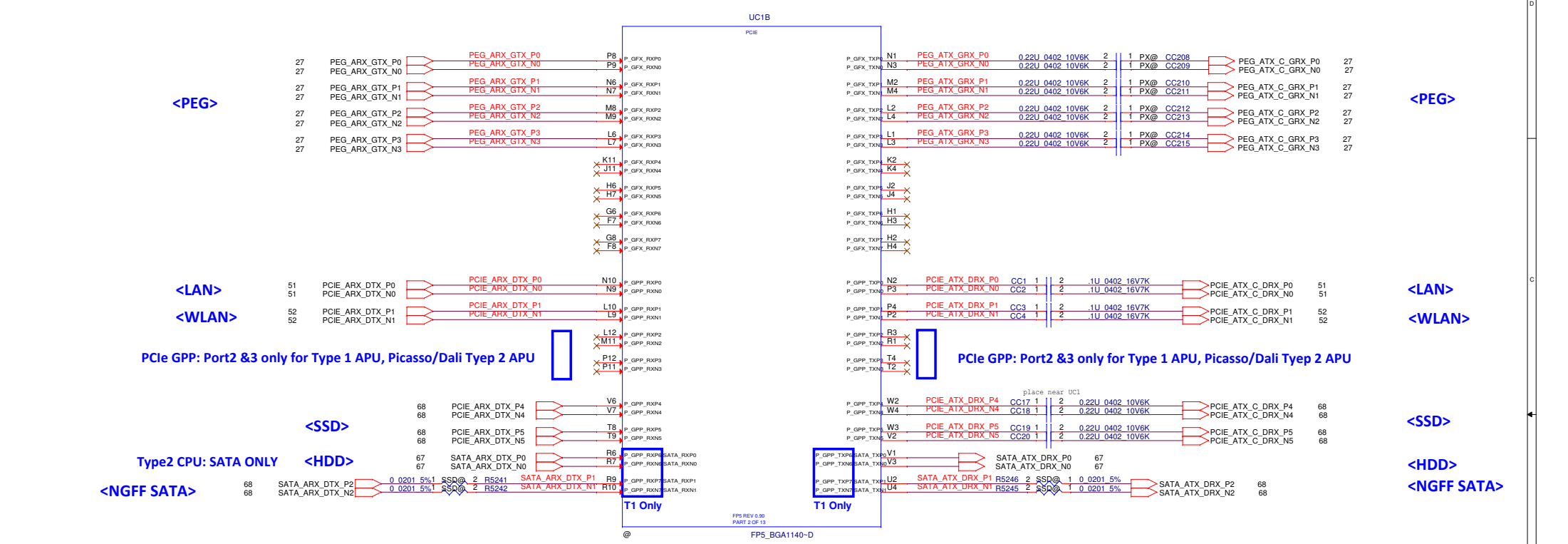
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X7677232L03	

777	MIC2_R3@
2G Micron	
X7677232L09	

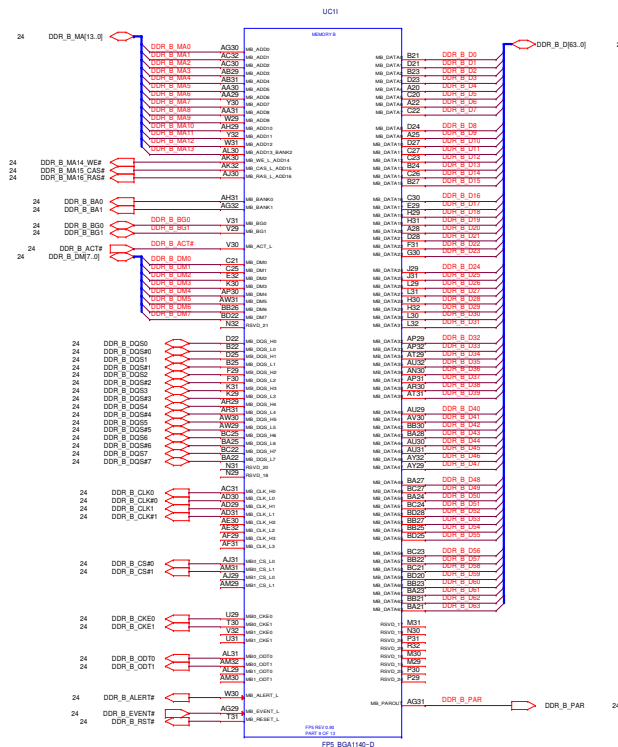
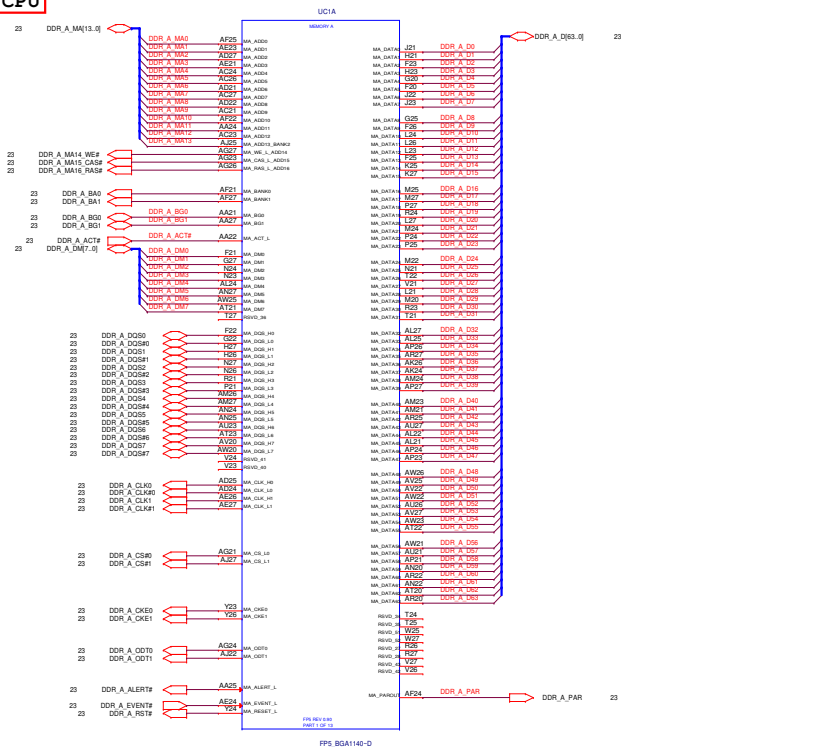
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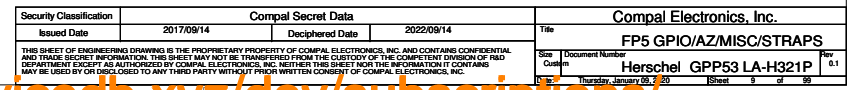
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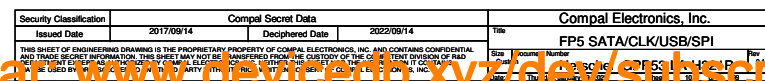




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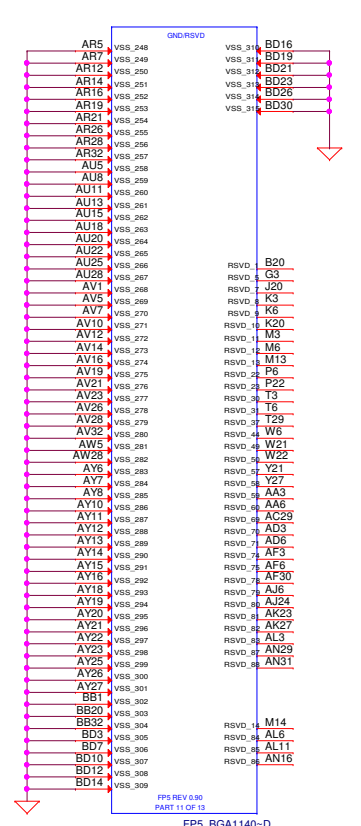
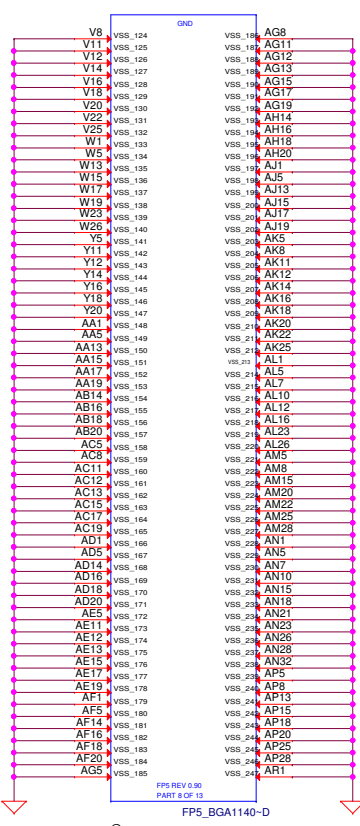
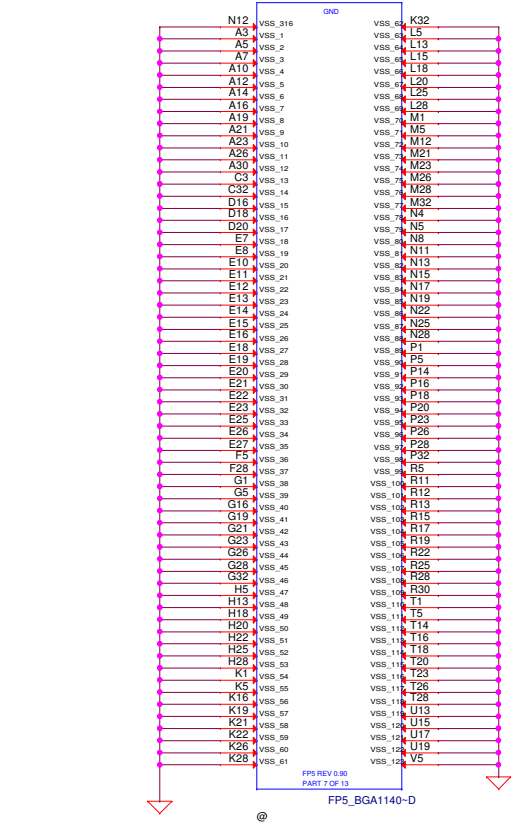


Main Func = CPU

UC1G

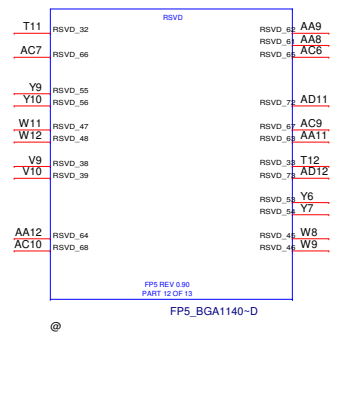
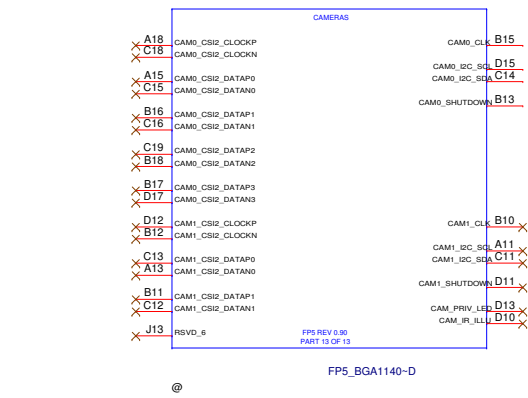
UC1H

UC1K



UC1M

UC1L



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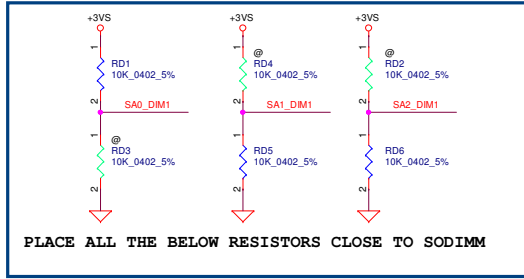
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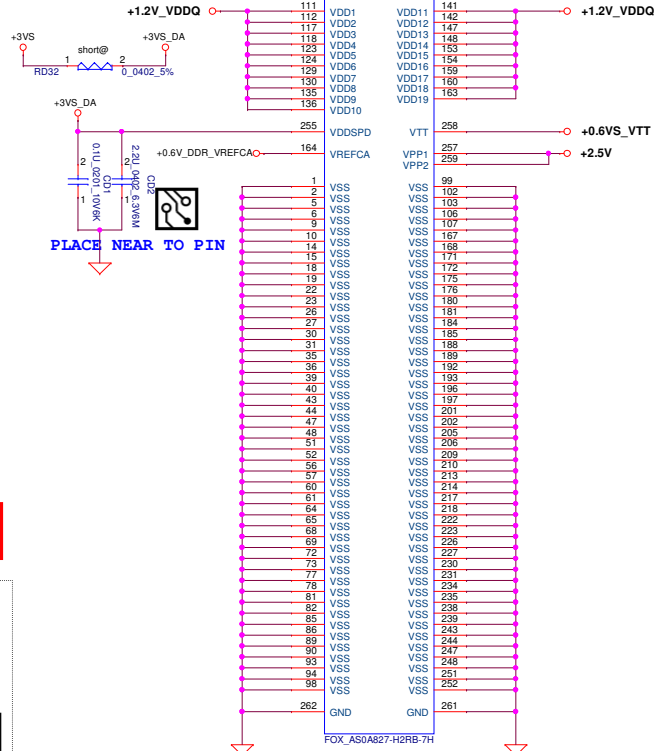
# Bristol CH-A REVERSE TYPE

## JDIMM1



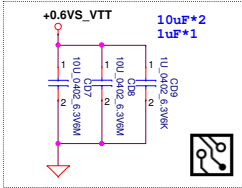
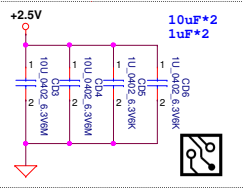
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL A :  
SA0 = 1; SA1 = 0; SA2 = 0.

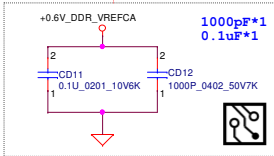


Layout Note:  
Place near JDIMM1.257,259

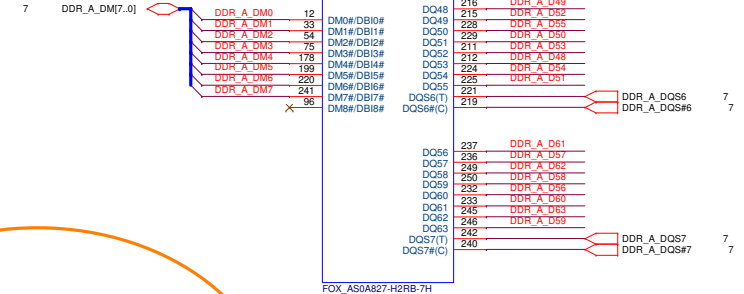
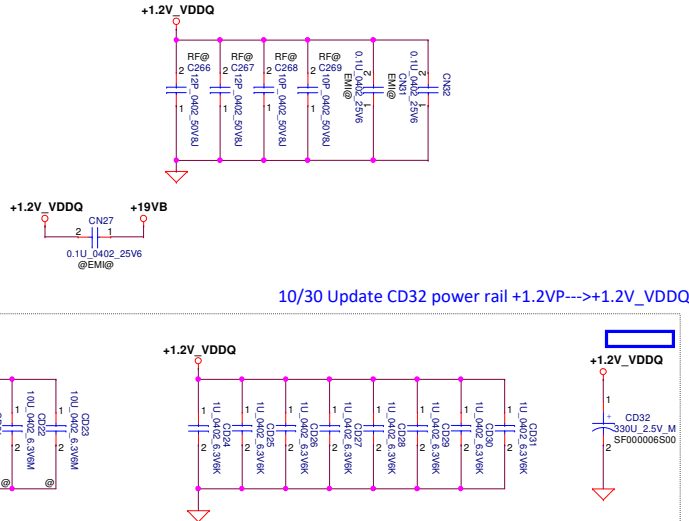
Layout Note:  
Place near JDIMM1.258



Layout Note:  
PLACE THE CAP near JDIMM1. 164

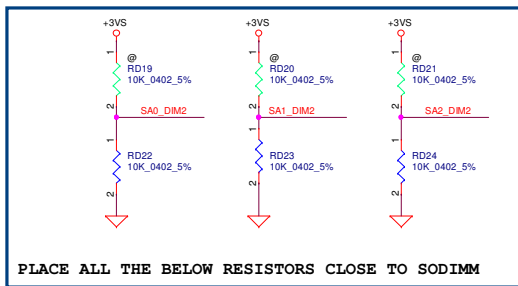


Layout Note:  
Place near JDIMM1

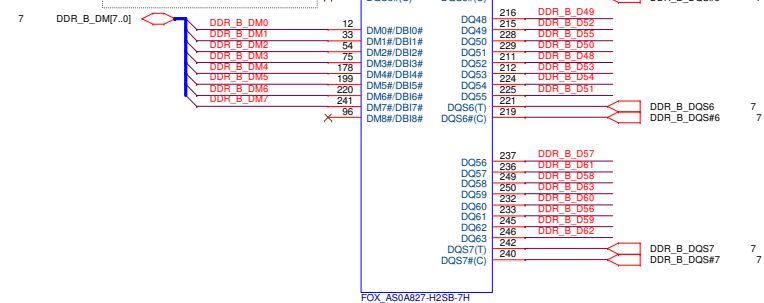
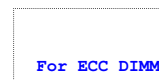
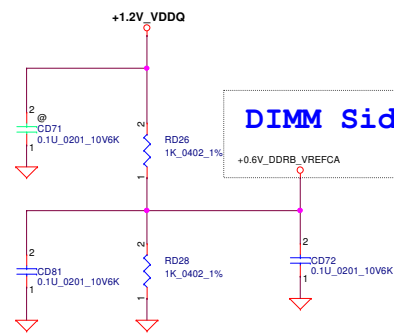
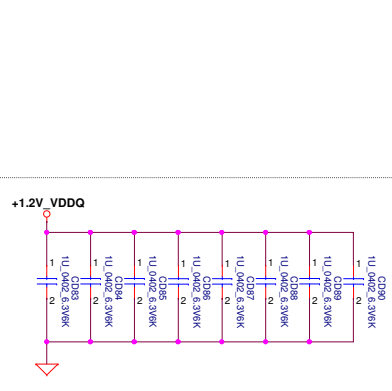
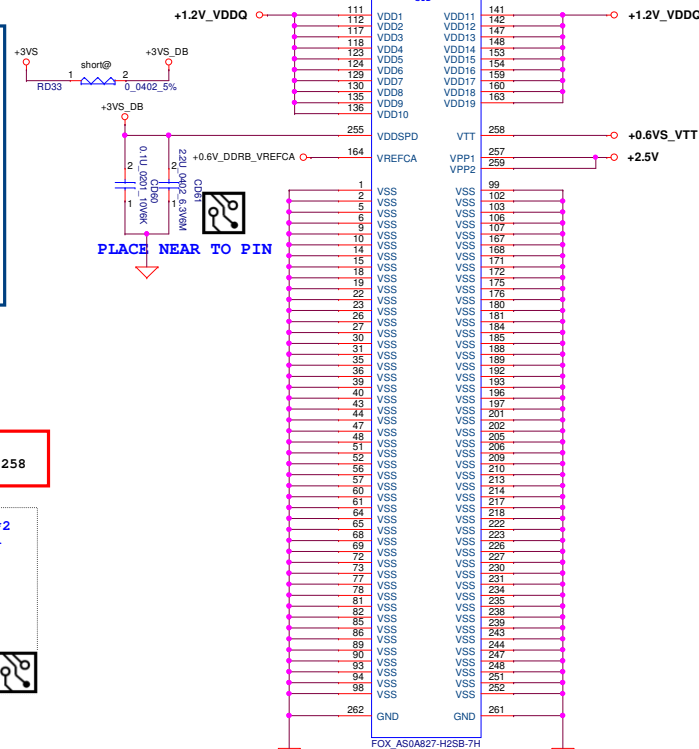
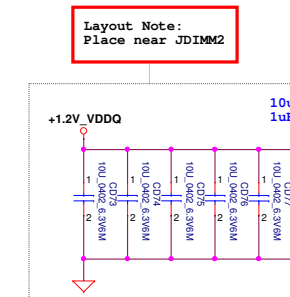
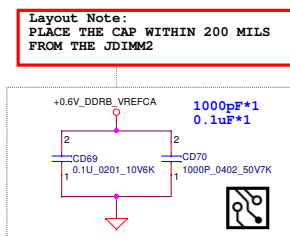
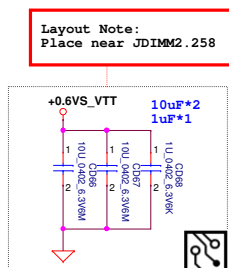
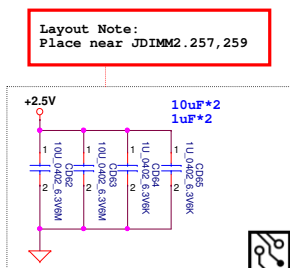


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Bristol CH-B STD  
JDIMM2



SPD ADDRESS FOR CHANNEL B :  
SA0 = 0; SA1 = 0; SA2 = 0.



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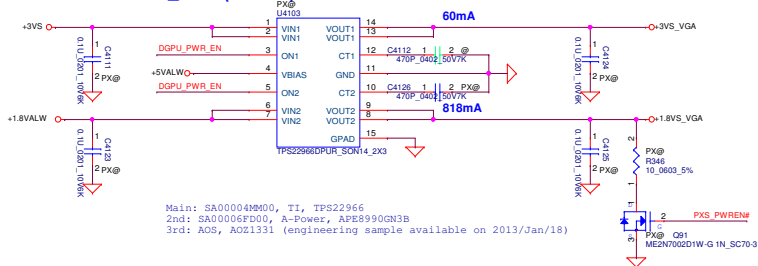
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					<b>Herschel GPP53 LA-H321P</b>
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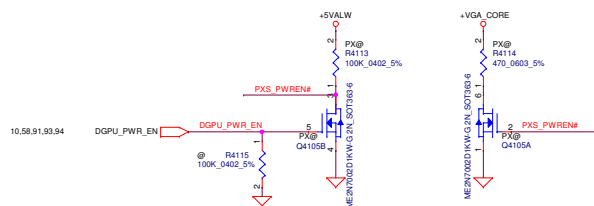
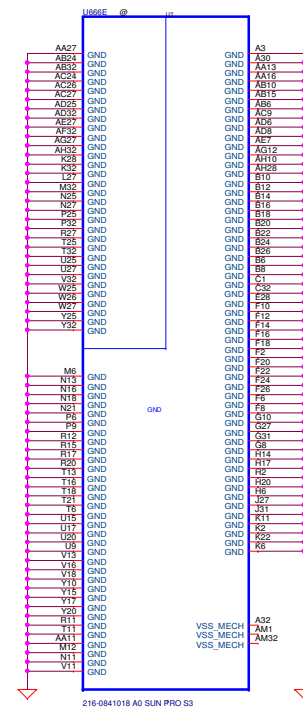
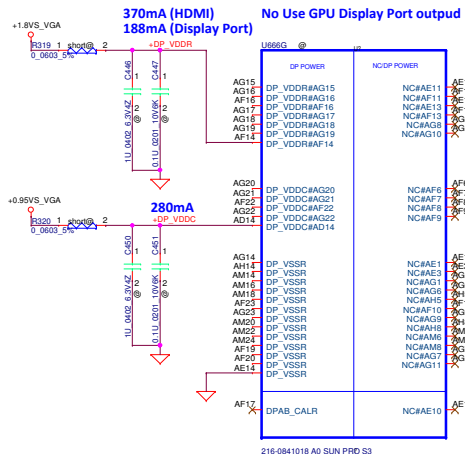
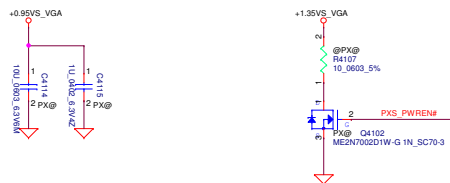




**+3VS to +3VS\_VGA (25mA)**  
**+1.8VALW to +1.8VS\_VGA (311mA)**



**+0.95VSG (2A)**



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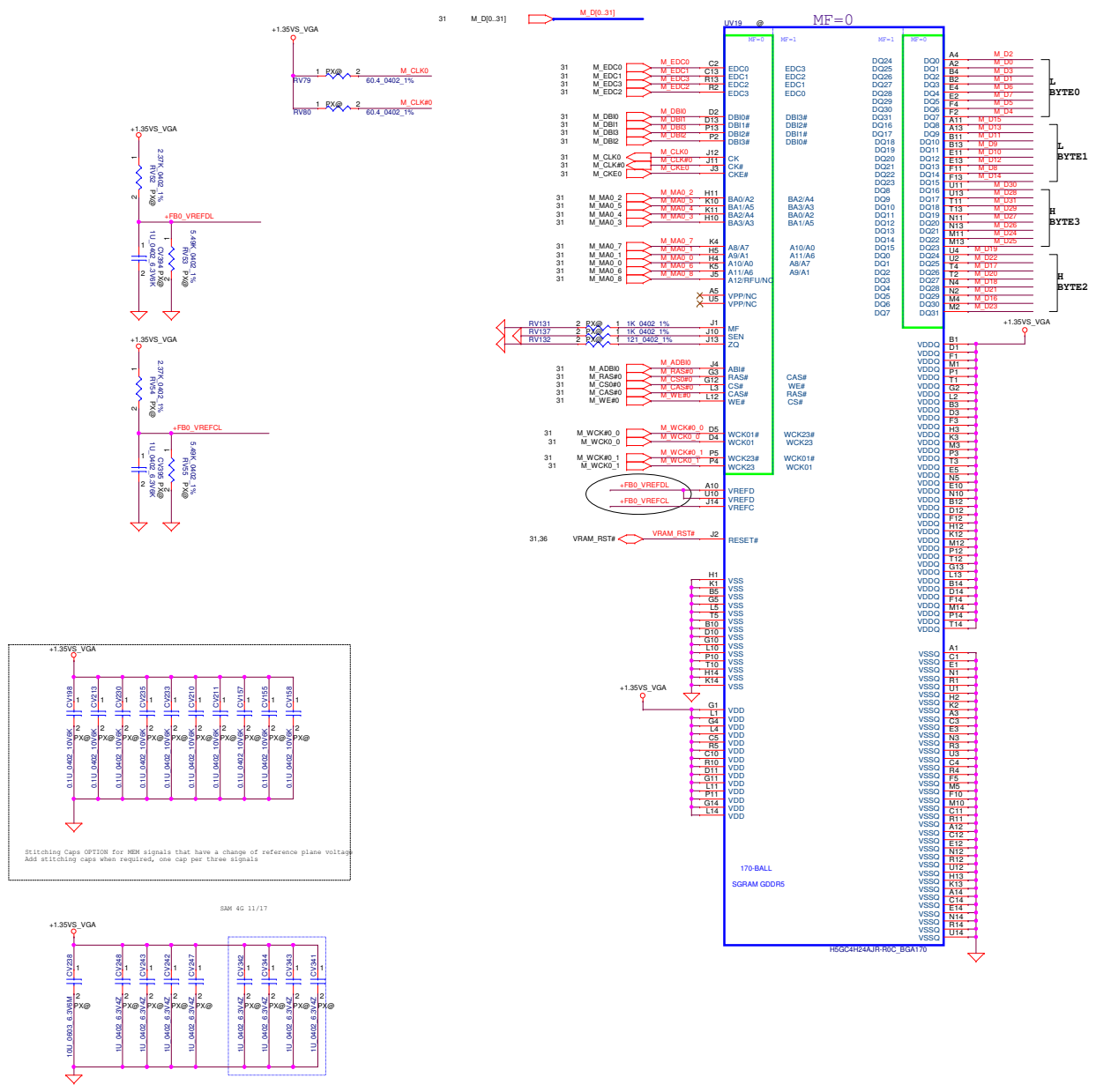


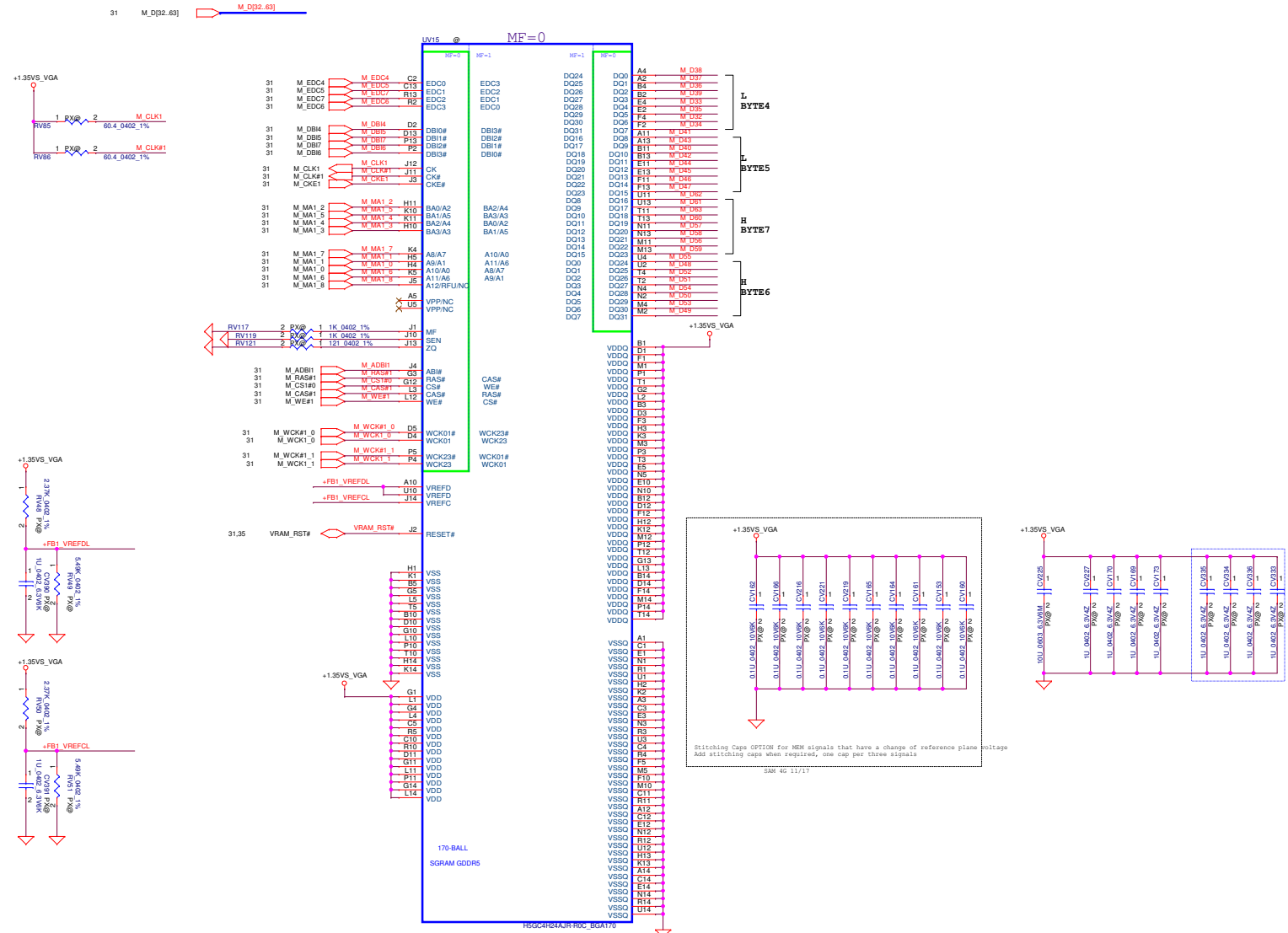
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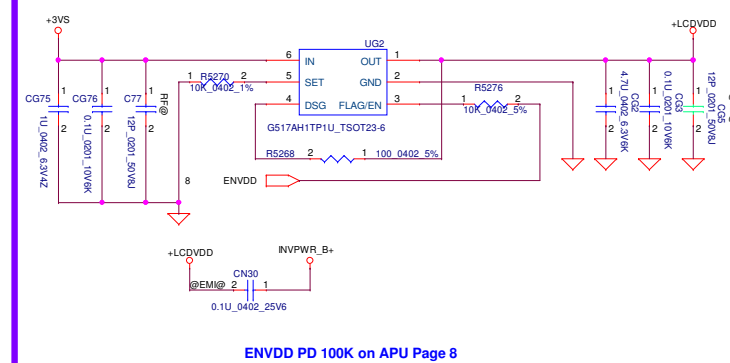
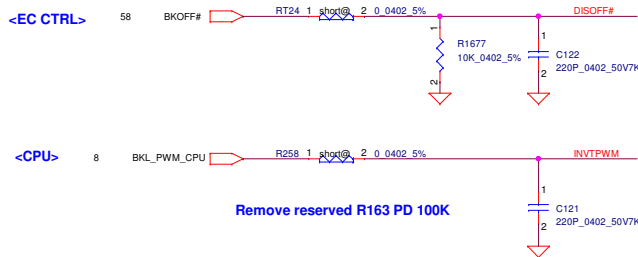
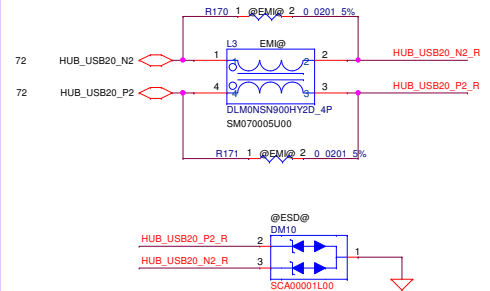
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[illegible]

**CC103~108 close JEDP <1000mil**

Pin	Signal	CC103	CC104	CC105	CC106	CC107	CC108
8	EDP_AUXP	1	2	1	2	1	2
8	EDP_AUXN	1	2	1	2	1	2
8	EDP_TXN0	1	2	1	2	1	2
8	EDP_TXP0	1	2	1	2	1	2
8	EDP_TXN1	1	2	1	2	1	2
8	EDP_TXP1	1	2	1	2	1	2

9 TS\_GPIO\_SOC

58 TS\_GPIO\_EC

R260 1 TS 2 0.0402 5%

R261 1 TS 2 0.0402 5%

Camera

R172 1 @EMI 2 0 0201 5%

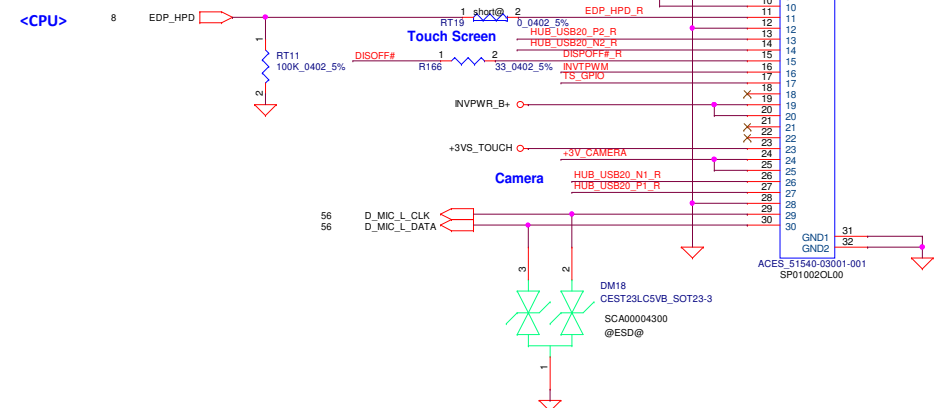
72 HUB\_USB20\_P1

72 HUB\_USB20\_N1

L12 EMI

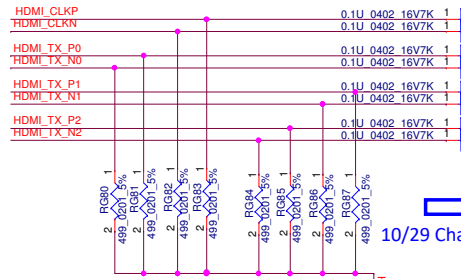
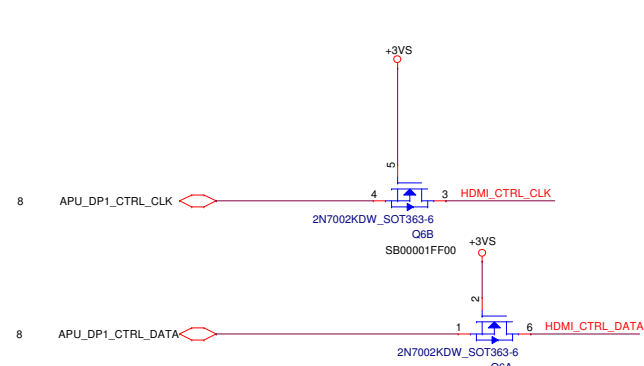
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R173 1 @EMI 2 0 0201 5%



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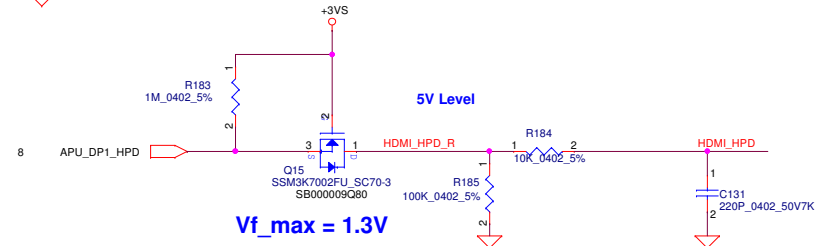
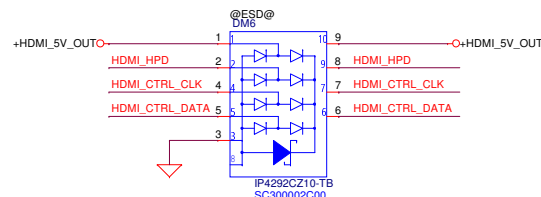
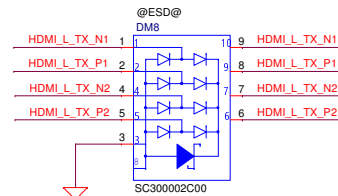
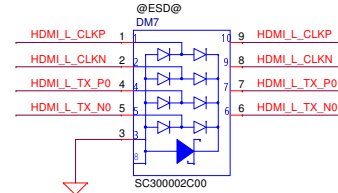
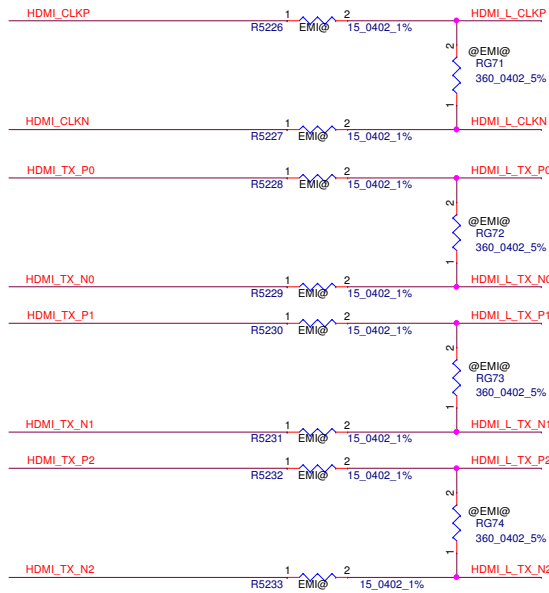
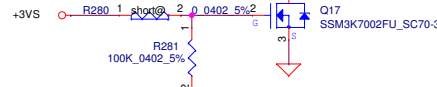
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10/29 Change RPH1 RPH2 to RG80-RG87 on HDMI signals

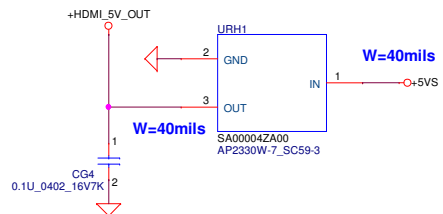
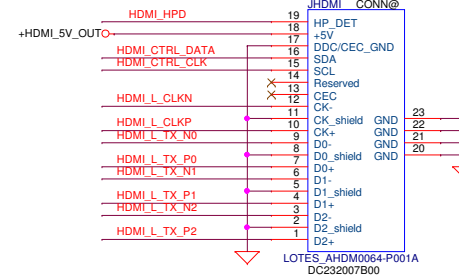
NET: HDMIRES\_GND  
WIDTH>20 mils

CLK  
Data0  
Data1  
Data2



Vf\_max = 1.3V

HDMI Conn.

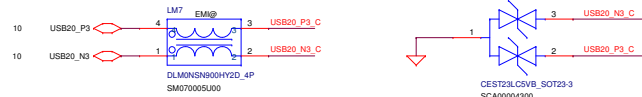
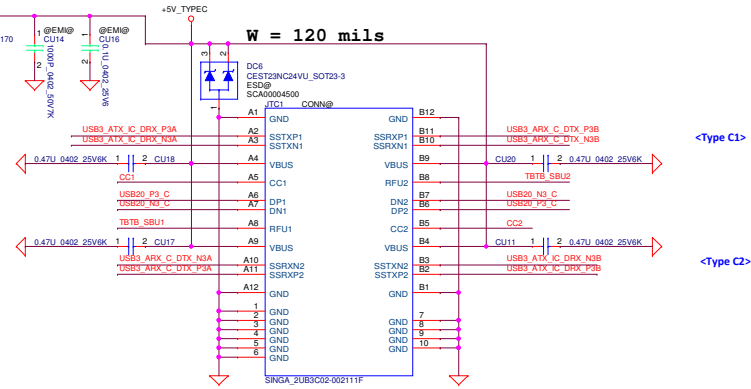
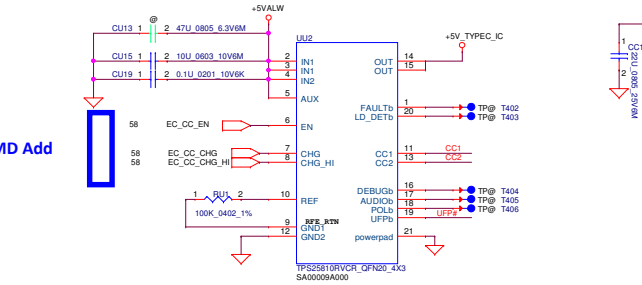




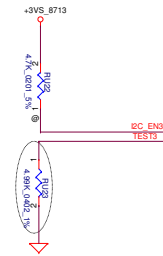
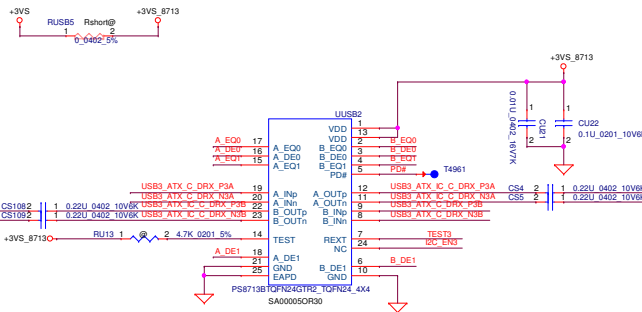
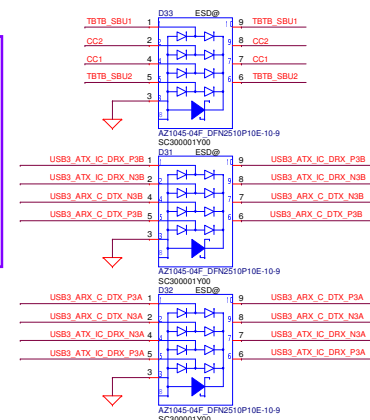
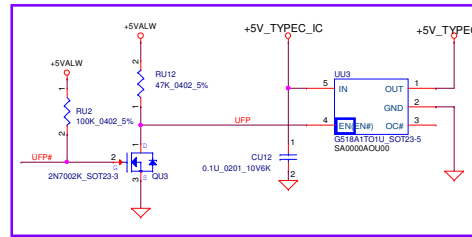
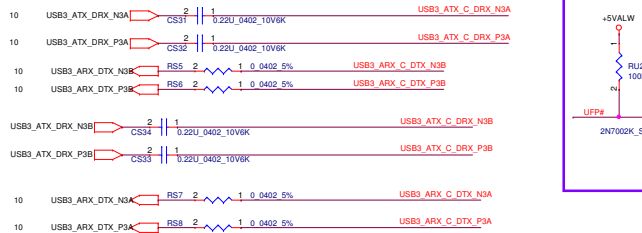
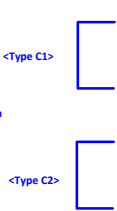
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# Type-C - USB only

2019 AMD Add



Follow Type C conn pin



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				Sheet	43 of 99



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						HW Reserve			
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							Design checked by: 2020/01/08		



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				Drawn Chen, Hui	Rev 0.1
				Sheet 48 of 99	



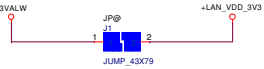


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				Drawn Chen, Hui	Rev 0.1
				Sheet 49 of 99	

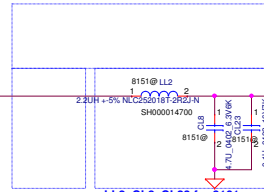


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				Sheet 50 of 99	

+LAN\_VDD\_3V3 Rising time  
need>0.5mS and <100mS



#### 8/15 Change to LDO Mode



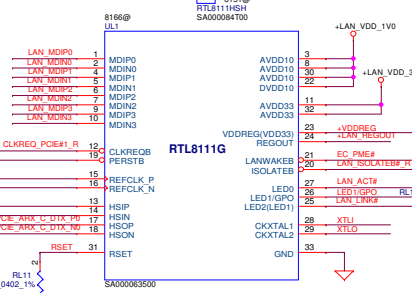
LDO mode	Switching mode
LL1 SMT	@
CL21 SMT	@
LL2 @	SMT
CL8,CL23@	SMT

CL13 & CL15 close UL1 Pin22  
CL14 & CL27 close UL1 Pin30

Place CL11-CL12 close UL1 Pin 3,8

LL2, CL8, CL23 for 8161  
CL8 & CL18 close LL2

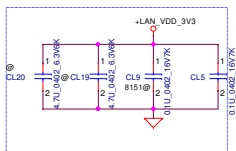
#### 8151/8166 Co-Lay



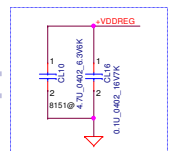
+LAN\_VDD\_3V3=40mil  
+VDDREG=40mil  
+LAN\_REGOUT=60mil



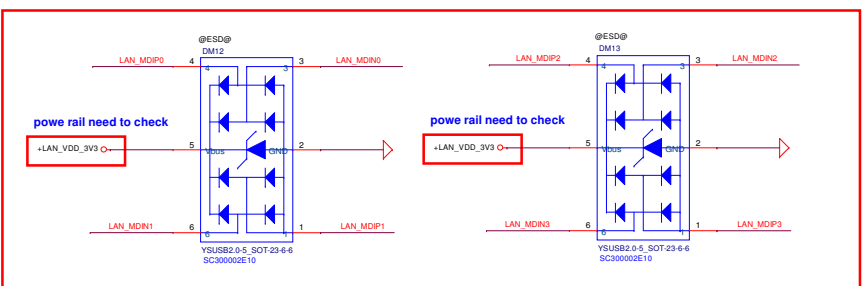
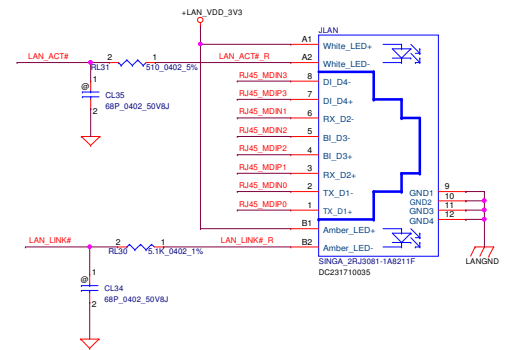
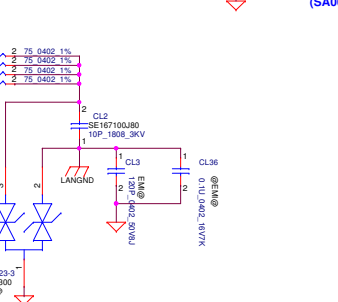
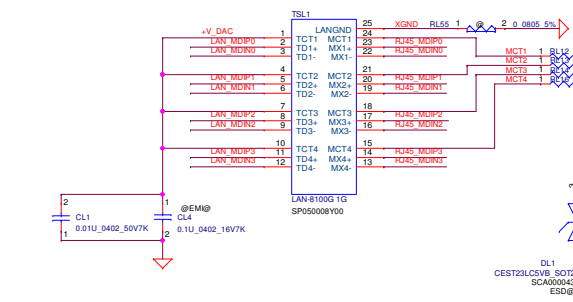
0923 PV CNG from DP00 to E500



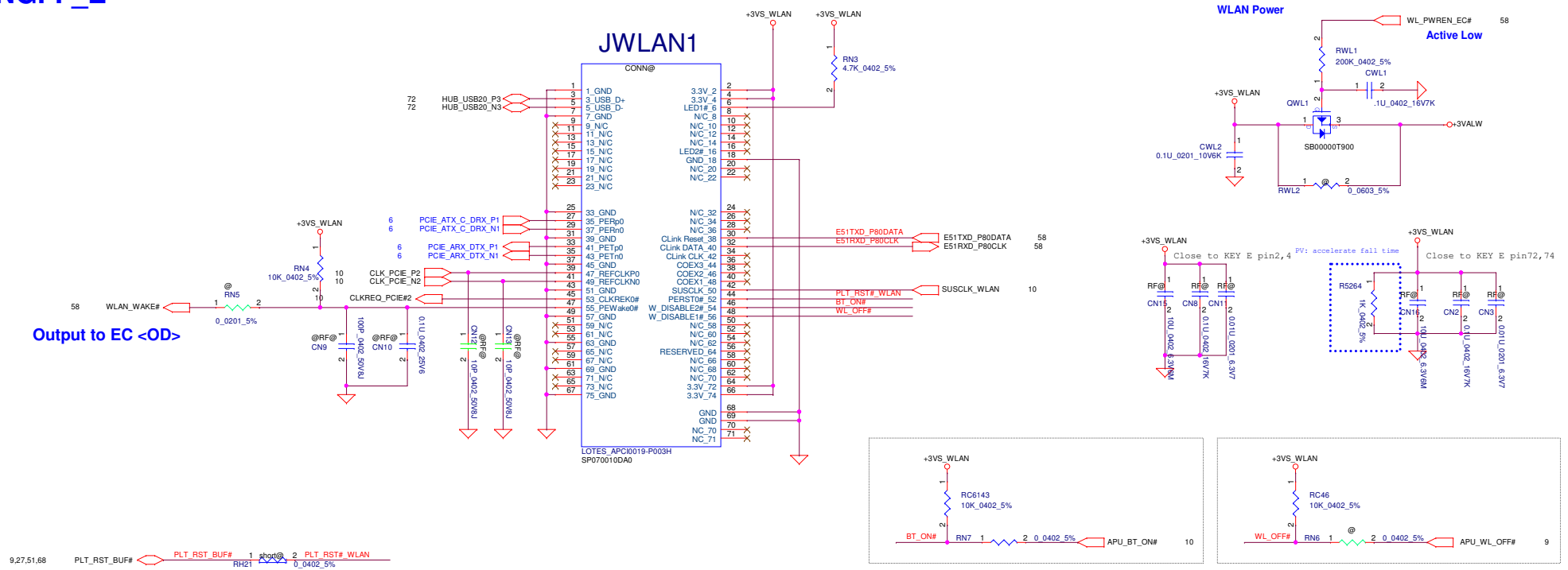
CL9 & CL5 close to UL1: Pin 11,32  
CL19 close to UL1: Pin 32  
CL20 close to UL1: Pin 11



CL10 & CL16 close to UL1: Pin 23



# WLAN NGFF\_E



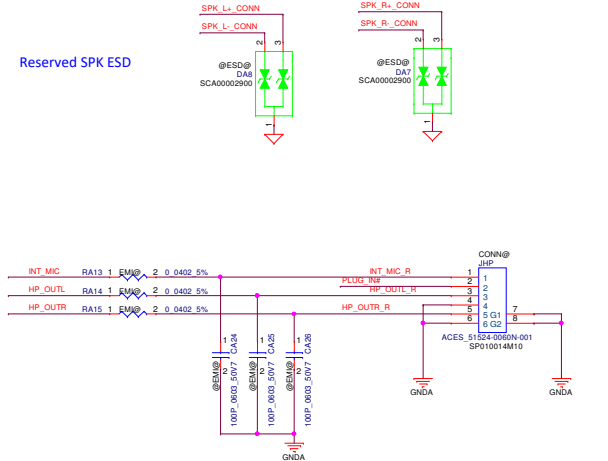
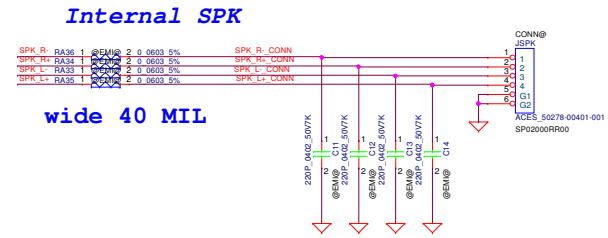
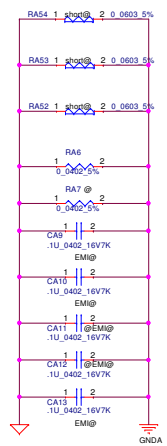
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				Rev	0.1

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				Date	Thursday, January 09, 2025
				Sheet	55 of 99
				Rev	0.1

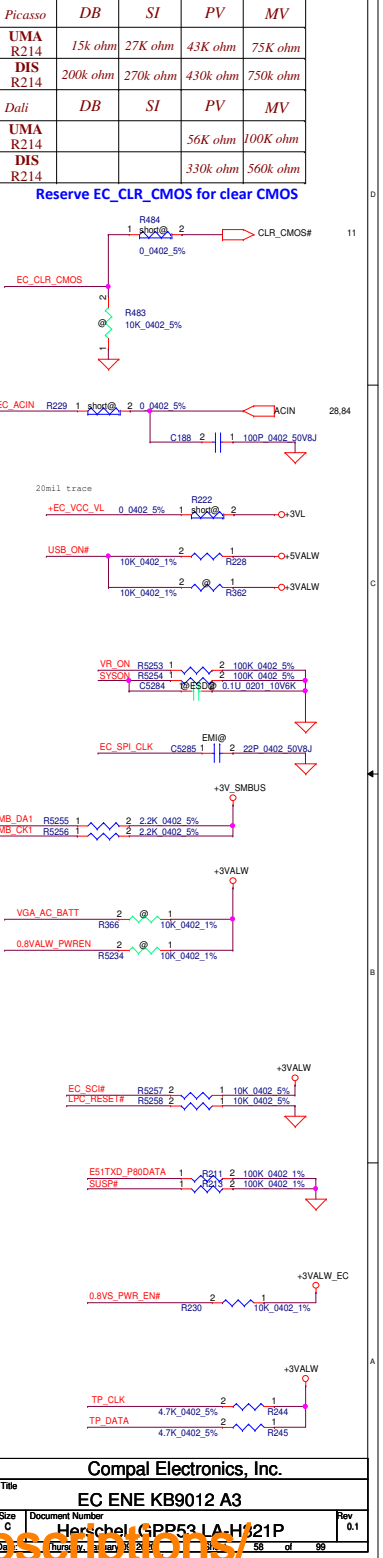
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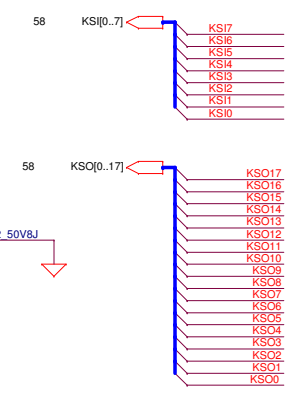
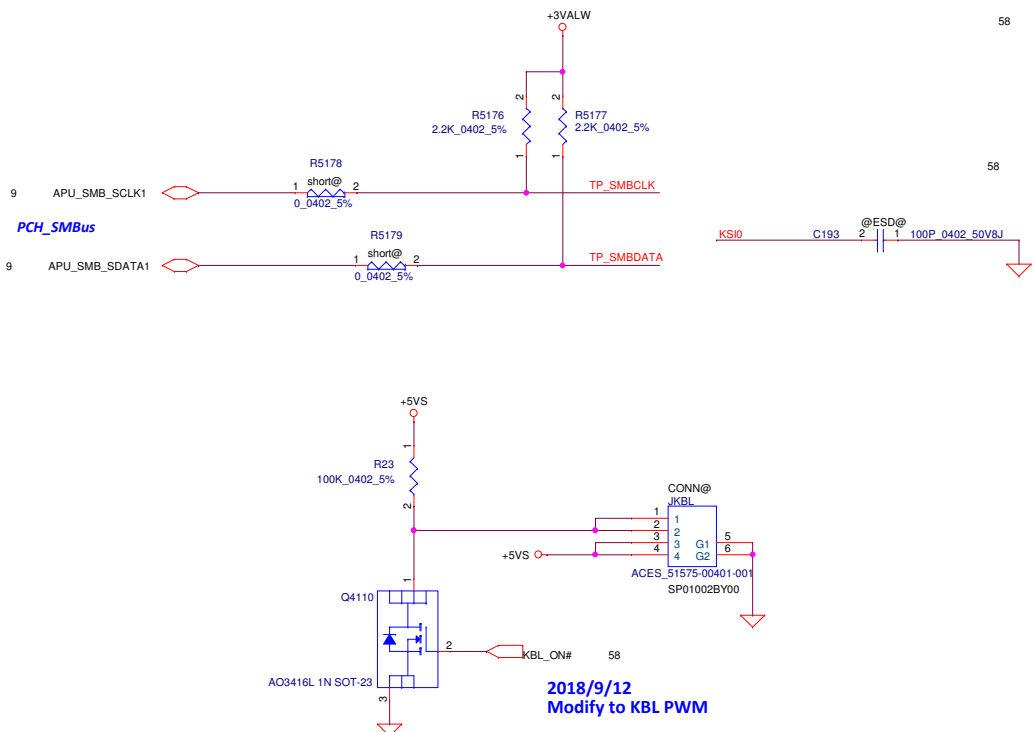


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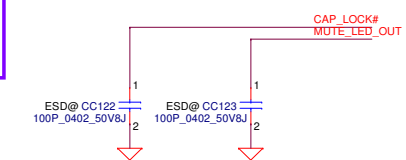
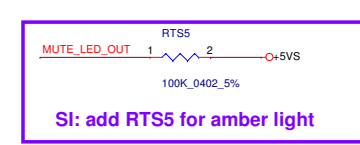
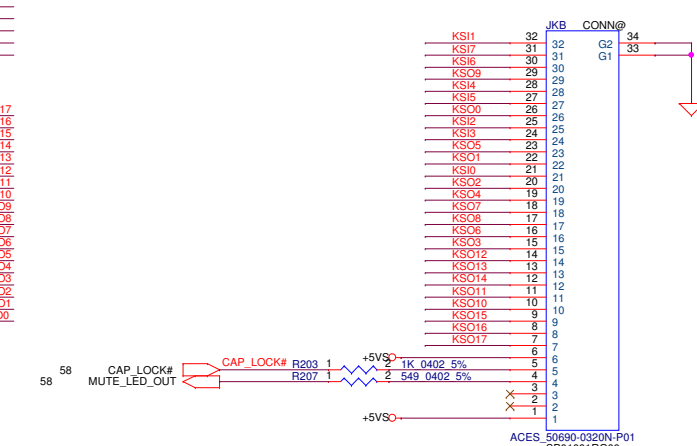
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				Date	Thursday, January 09, 2020
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					Herschel GPP53 LA-H321P
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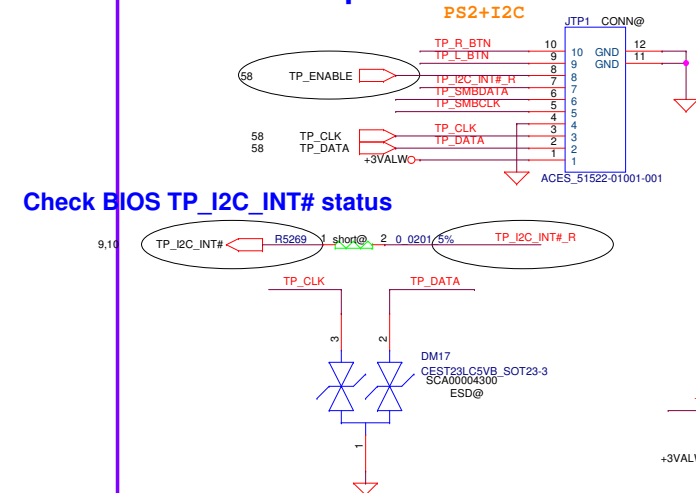
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				Date	Thursday, January 09, 2020
				Sheet	62 of 99
				Rev	0.1



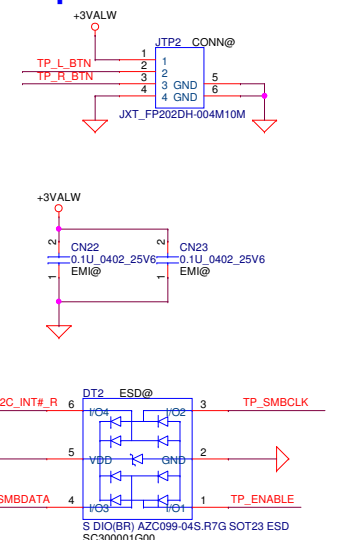
## Keyboard conn



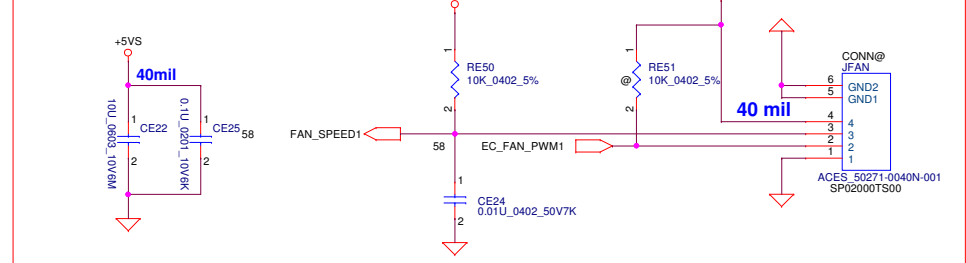
## 10 pin to TP Module



## 4 pin to TP S/B



## FAN conn

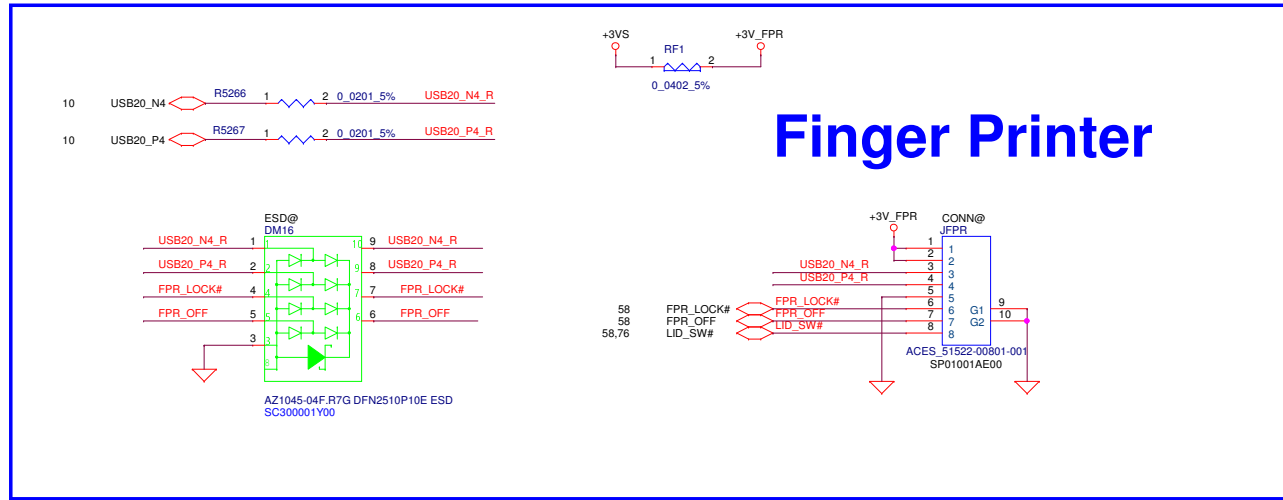
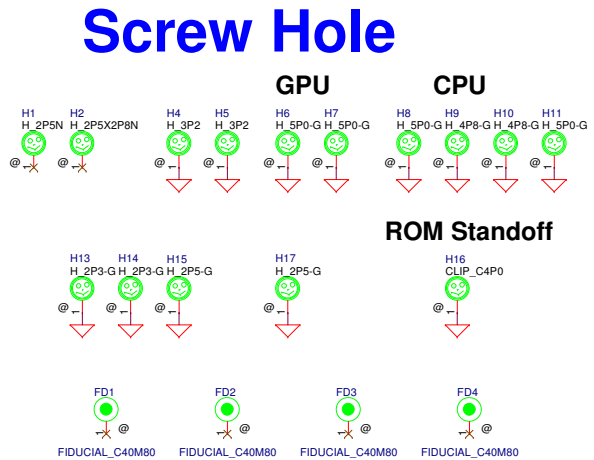
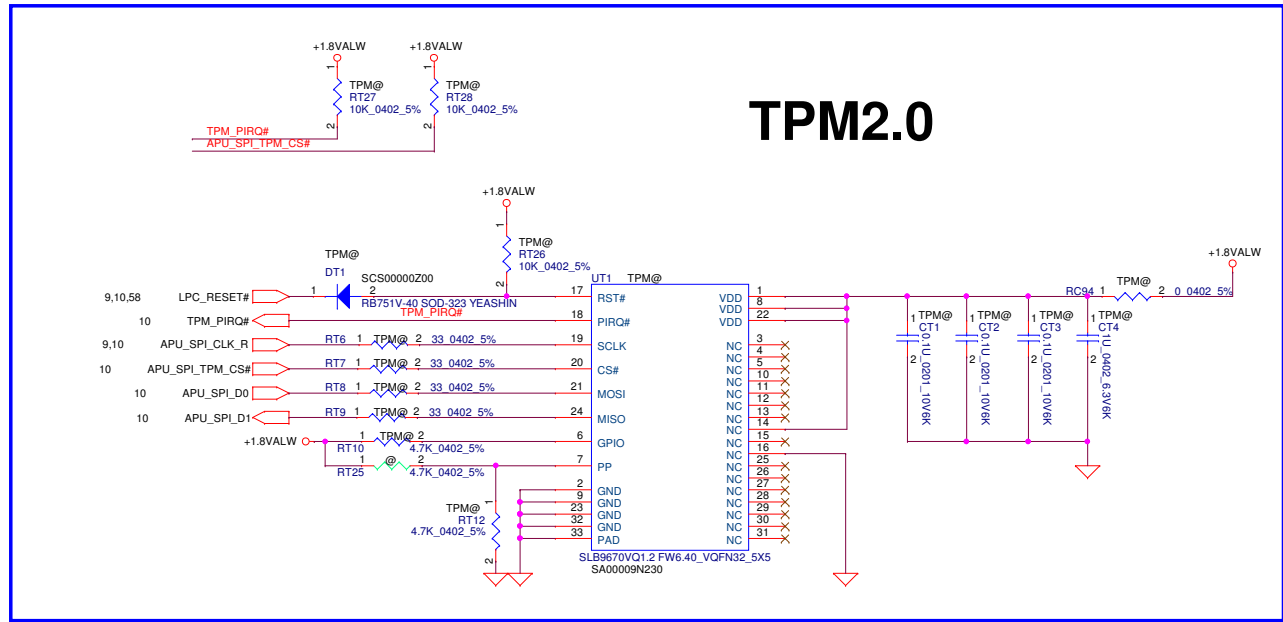


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					<b>Herschel GPP53 LA-H321P</b>
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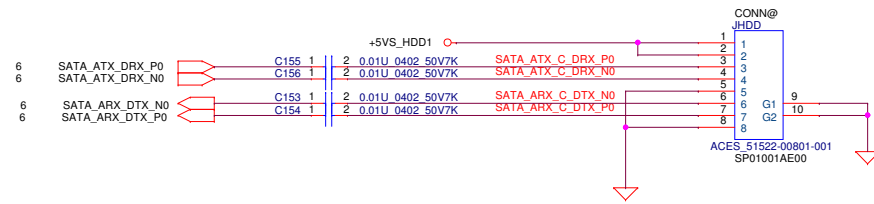
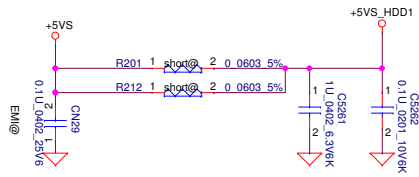


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					<b>Herschel GPP53 LA-H321P</b>
				Drawn	Thursday, January 09, 2020
				Sheet	65 of 99
				Rev	0.1

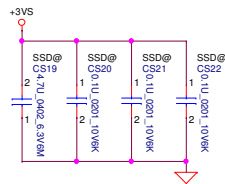


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				File: 010120170914_001	1 Sheet 66 of 99

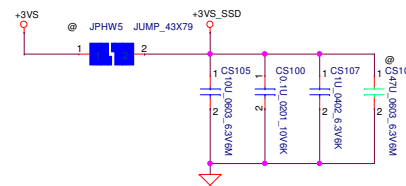
2.5" SATA HDD connector



# SSD



JPHW5 need to short



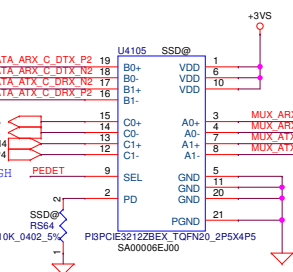
CPU

SATA\_ARX\_DTX\_P2  
SATA\_ARX\_DTX\_N2  
SATA\_ATX\_DRX\_N2  
SATA\_ATX\_DRX\_P2

CPU

SSD@ CS101 1  
SSD@ CS102 1  
SSD@ CS104 1  
SSD@ CS103 1

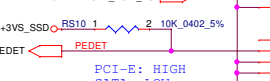
PCI-E: HIGH  
SATA: LOW



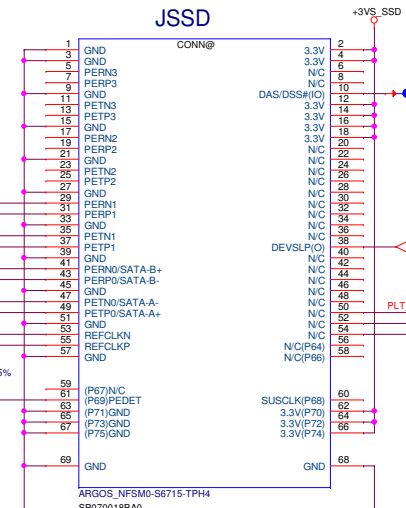
MUX

PCIE\_ARX\_DTX\_N5  
PCIE\_ARX\_DTX\_P5  
PCIE\_ATX\_C\_DRX\_N5  
PCIE\_ATX\_C\_DRX\_P5

MUX\_ARX\_C\_DTX\_NP  
MUX\_ARX\_C\_DTX\_PN  
MUX\_ATX\_C\_DRX\_NN  
MUX\_ATX\_C\_DRX\_PP



JSSD

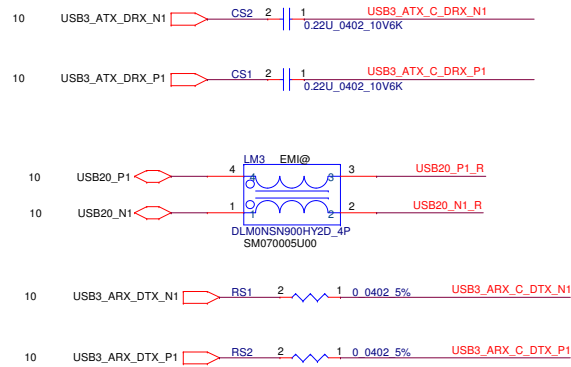


## Truth Table

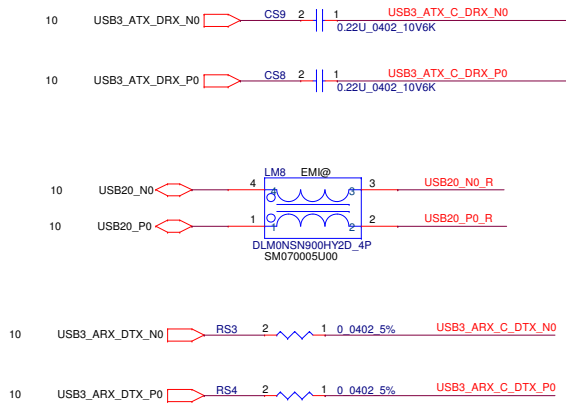
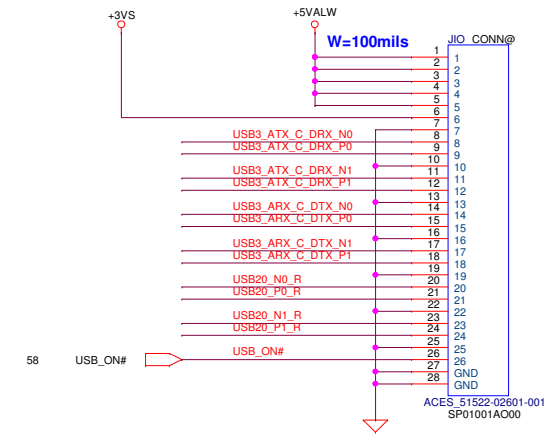
Function	SEL	PD
A to B	L	L
A to C	H	L
All ports Hi-Z, IC Power Down	X	H

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				Date	Thursday, January 09, 2020
				Sheet	69 of 99
				Rev	0.1

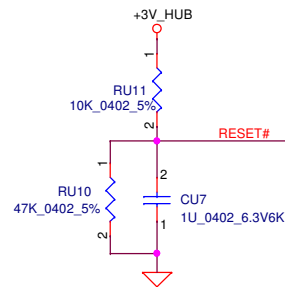
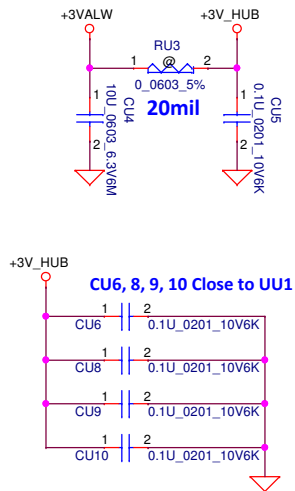
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USB3.0 port x 2



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				Document Number		Herschel GPP53 LA-H321P	
Customer		Herschel GPP53 LA-H321P		Rev		0.1	
Date		11/3/2017		U1		U2	
Sheet		71		of		99	



**CPU**

RESET#

RU5 1 2 680 0402 1% RREF

USB20\_N5

USB20\_P5

10 10

2 680 0402 1% RREF

PSELF

PGANG

OVCUR1#

OVCUR2#

XTAL\_HUB\_12M\_IN

XTAL\_HUB\_12M\_OUT

6 7

XIN XOUT

15

GND

GL850S-HHY22\_SSOP28

SA00007Q480

DM0 DP0

AVDD2 AVDD3

DVDD V5

V33

DM1 DP1

DM2 DP2

DM3 DP3

DM4 DP4

PWREN1# PWREN2#

27 28

HUB\_USB20\_N1

HUB\_USB20\_P1

HUB\_USB20\_N2

HUB\_USB20\_P2

HUB\_USB20\_N3

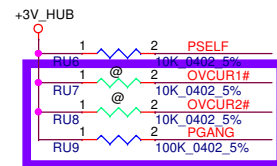
HUB\_USB20\_P3

38 38 38 38 52 52

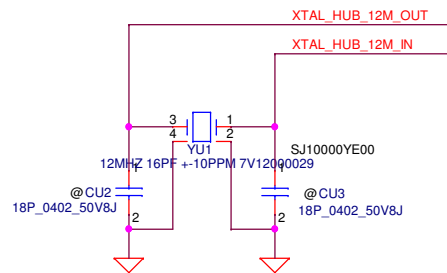
<Camera>

<Touch Screen>

<BT>



DB: change PGANG to PU for Gang mode  
Unpop RU6&7 for unuse OCP



Vender review:CU2, CU3 cap no install

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				Date:	Thursday, January 09, 2020
				Sheet	72 of 99



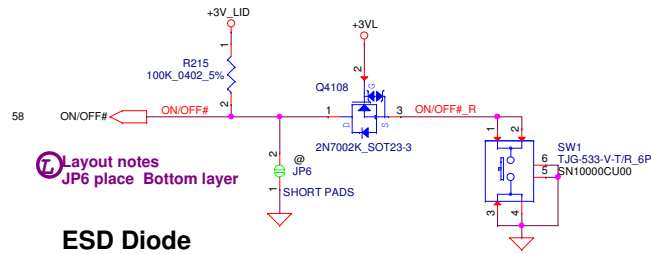


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				Herschel GPP53 LA-H321P	0.1
				1 Sheet	73 of 99

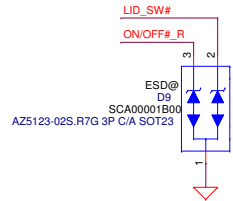
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				Date	Thursday, January 09, 2020
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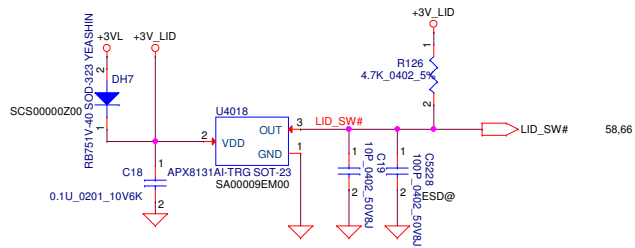
## Power Button Switch



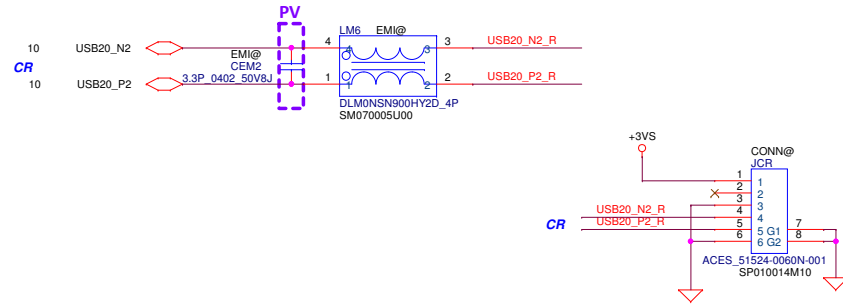
## ESD Diode



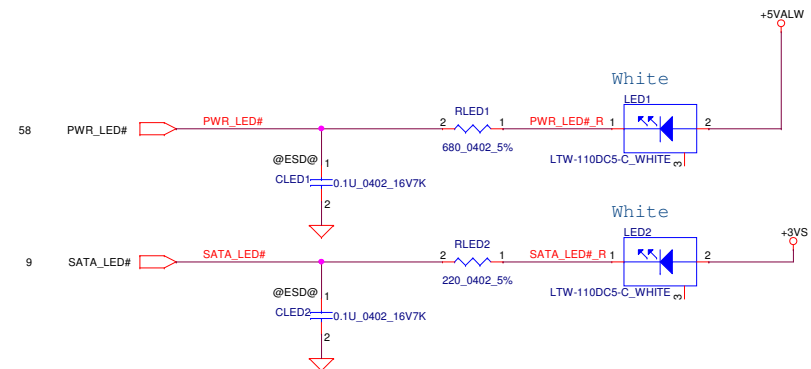
## Lid Switch (Hall Effect Sensor)



## JIO S/B



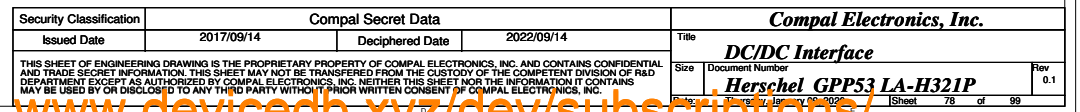
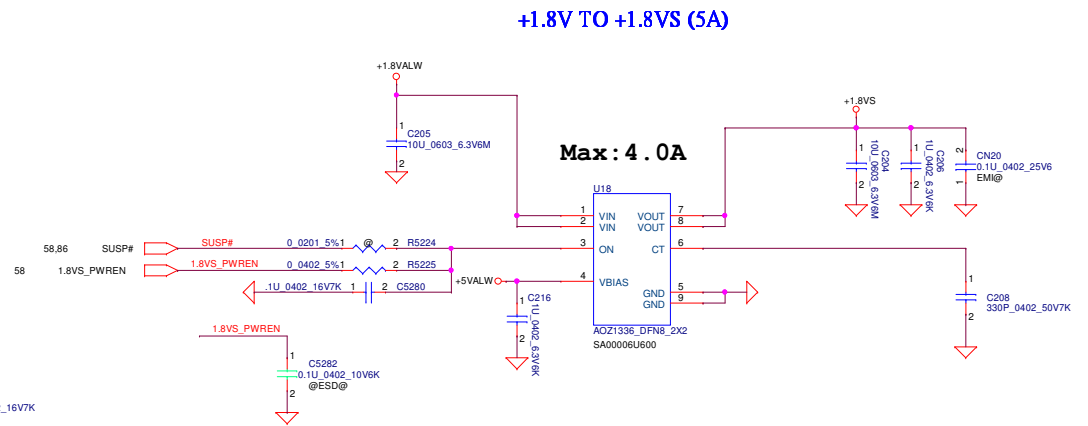
## HDD LED/ POWER LED



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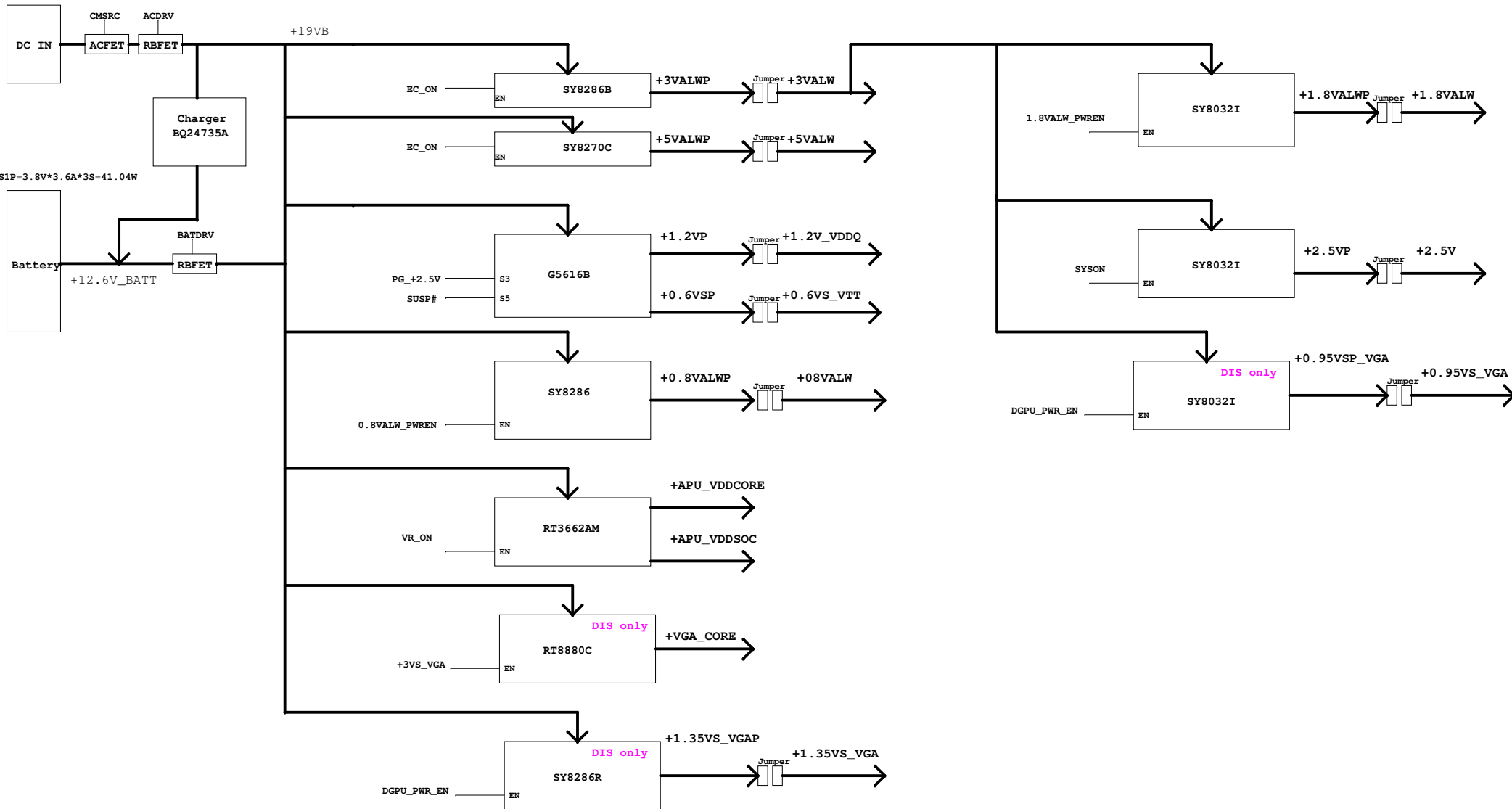


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				Date	Thursday, January 09, 2020
				Sheet	60 of 50
				Rev	0.1

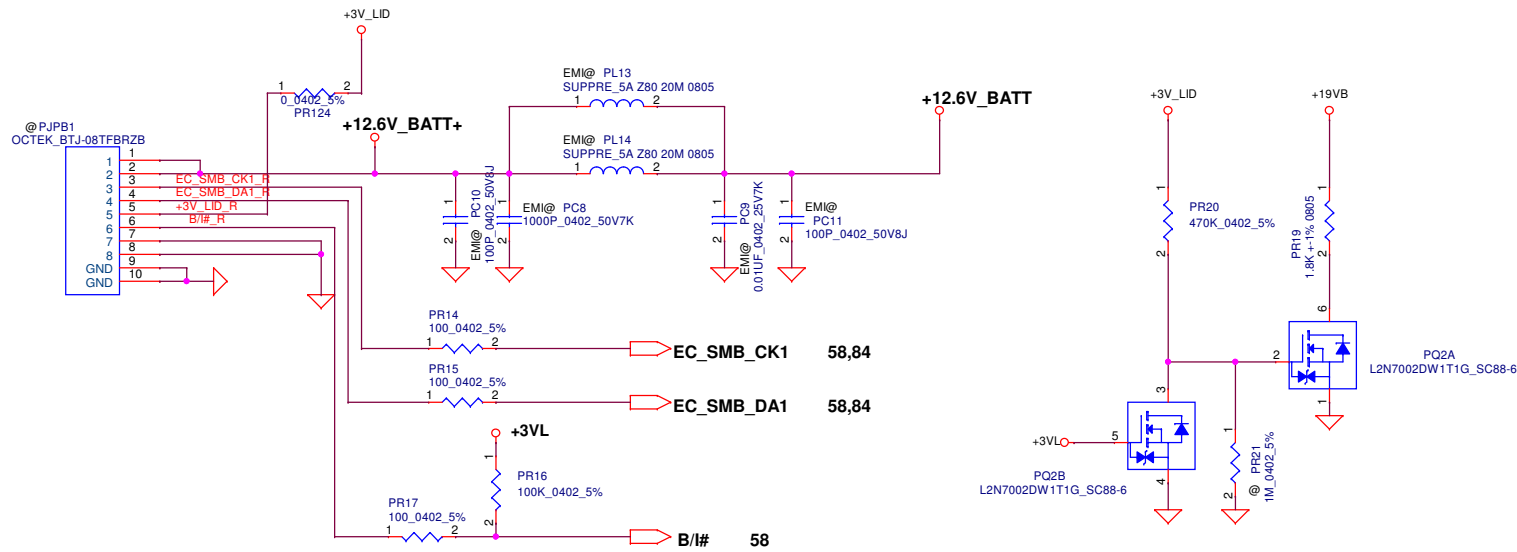


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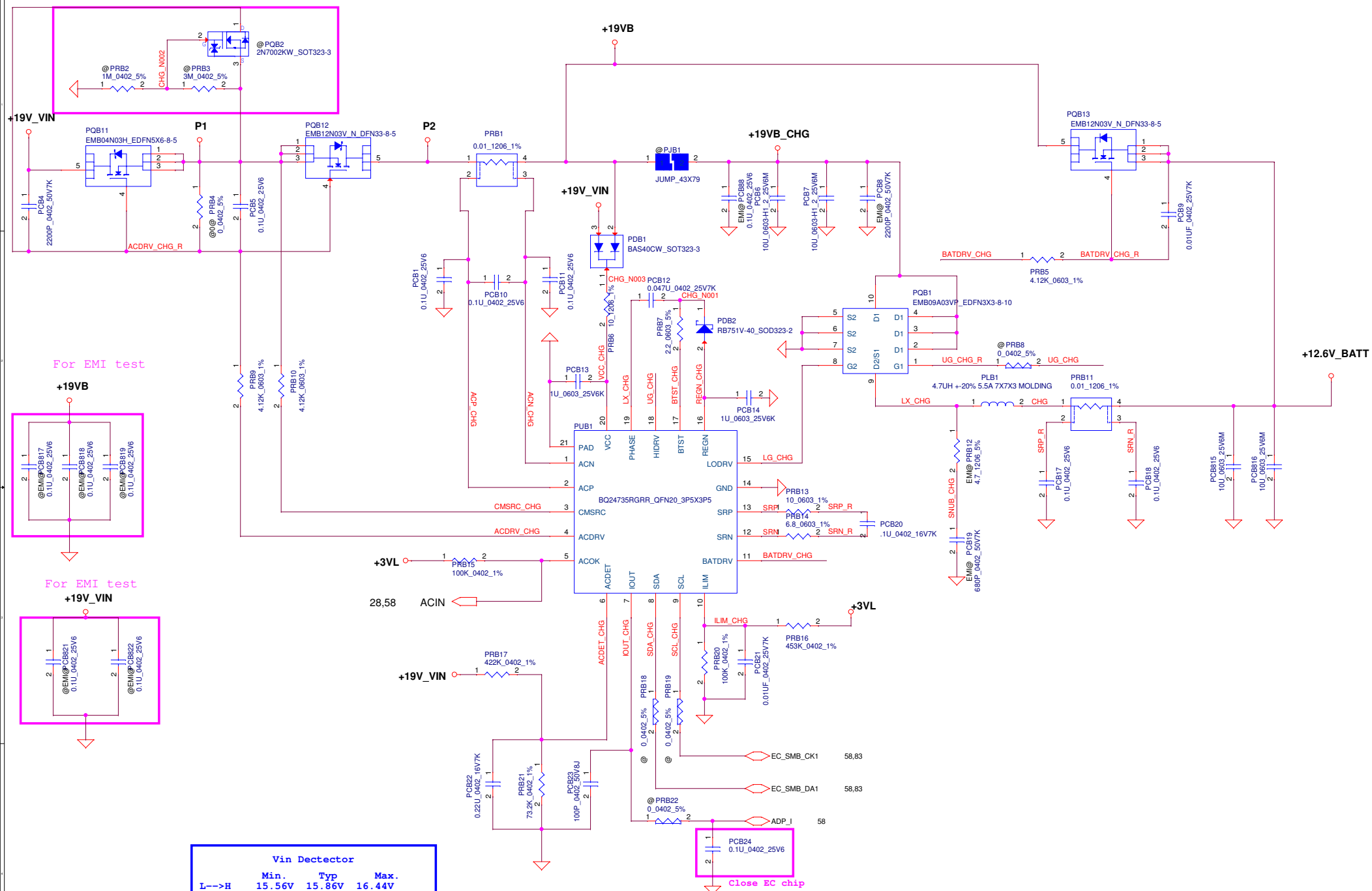
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Protection for reverse input

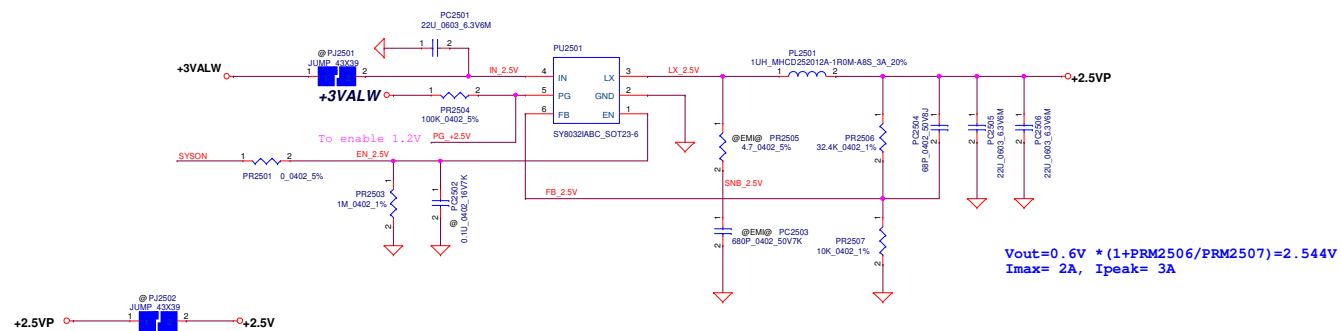
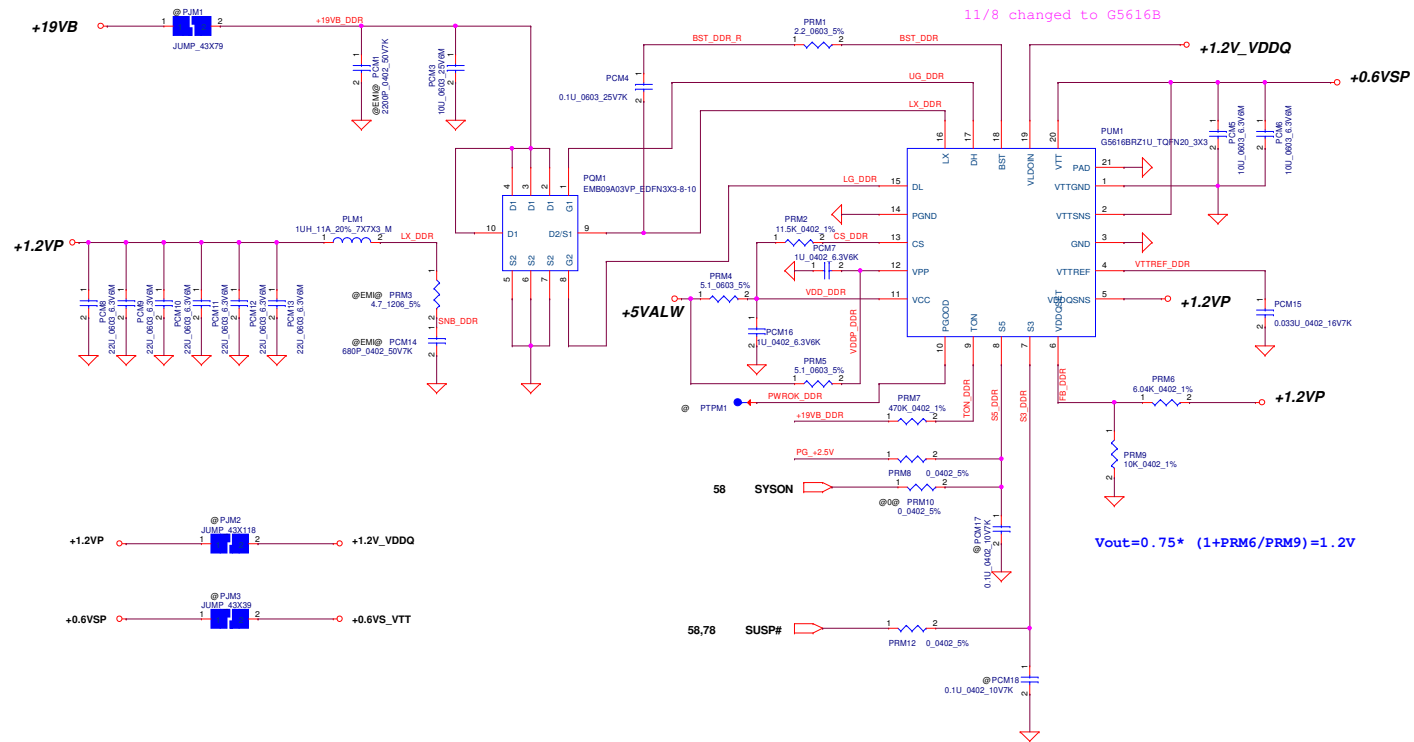


Vin Detector			
	Min.	Typ	Max.
L-->H	15.56V	15.86V	16.44V
H-->L	15.16V	15.46V	16.04V

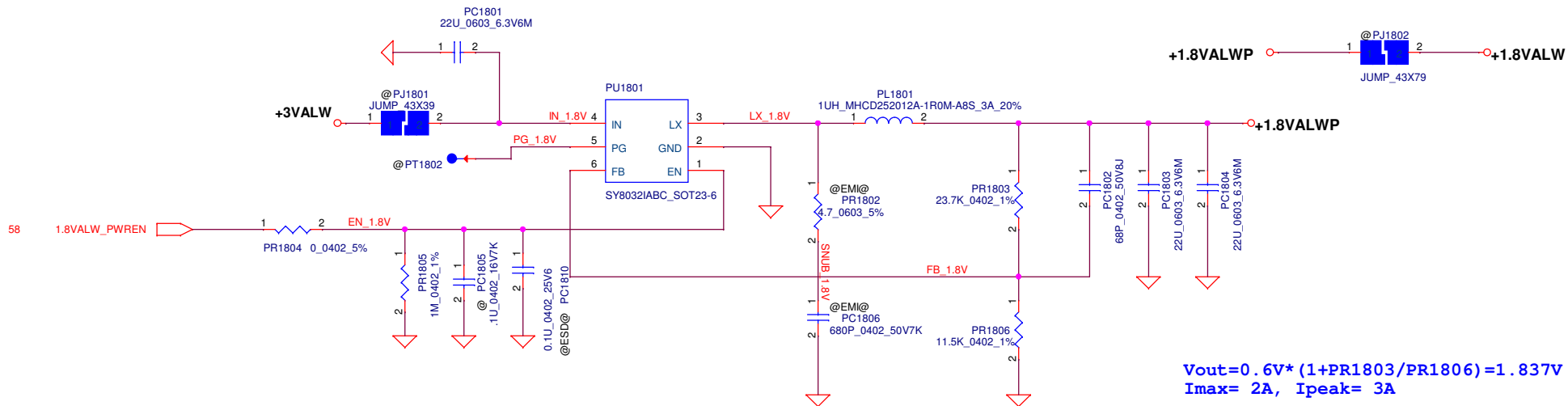
$V_{ILIM} = 20 * I_{LIM} * R_{sr}$   
 $I_{LIM} = 3.3 * 100 / (100 + 620) / 20 / 0.02$   
 $= 2.291 A$

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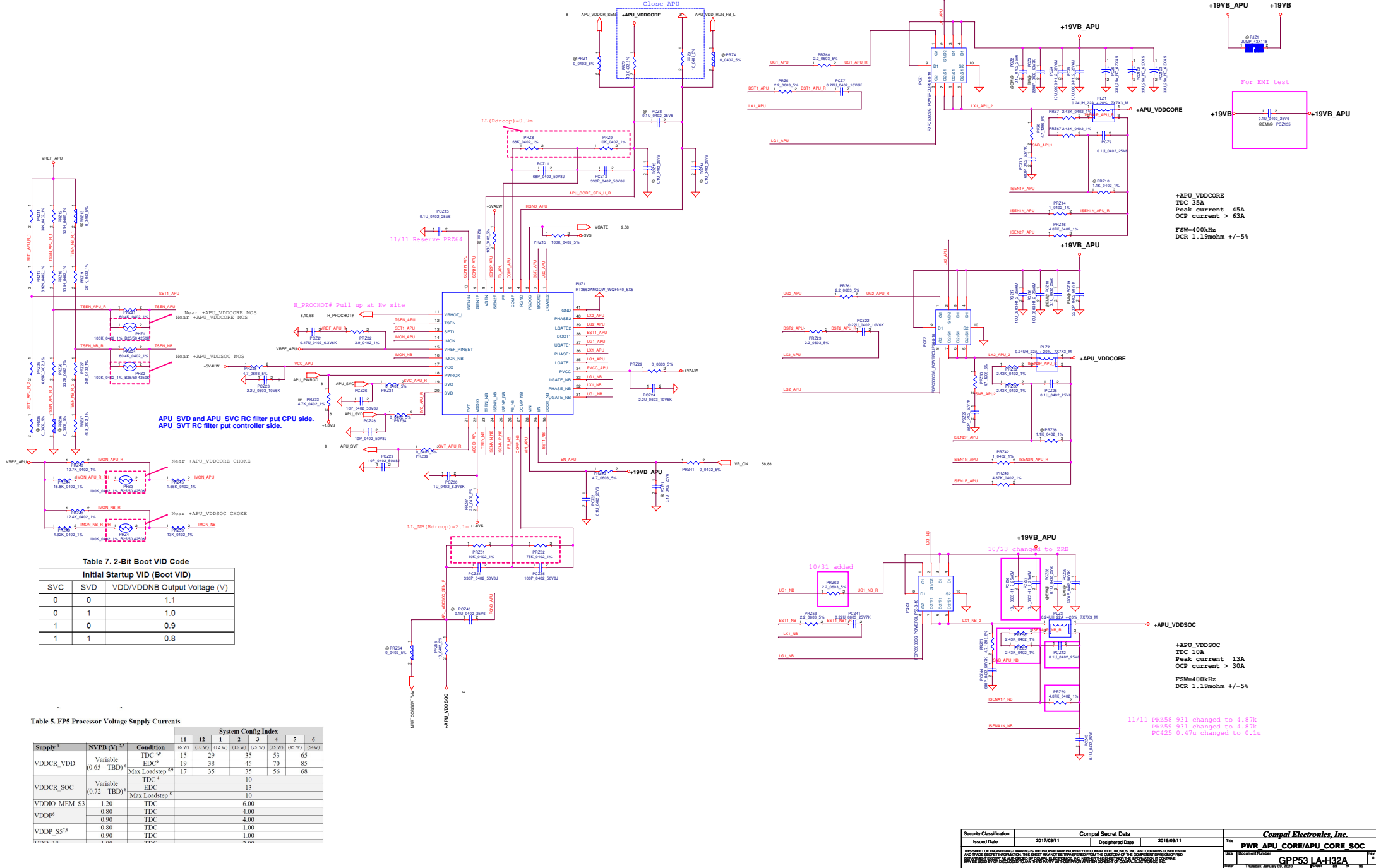
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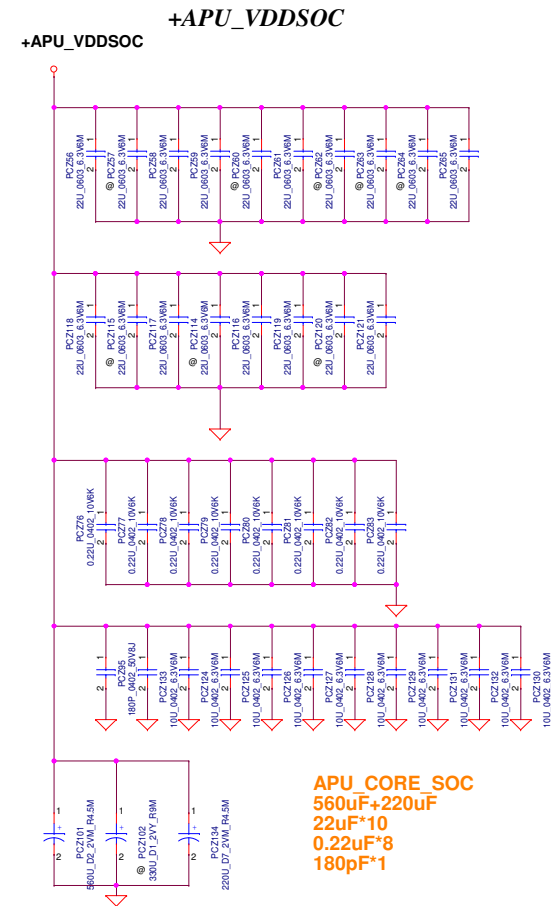


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				GPP53 LA-H32A	0.1
				Date:	Sheet 87 of 99



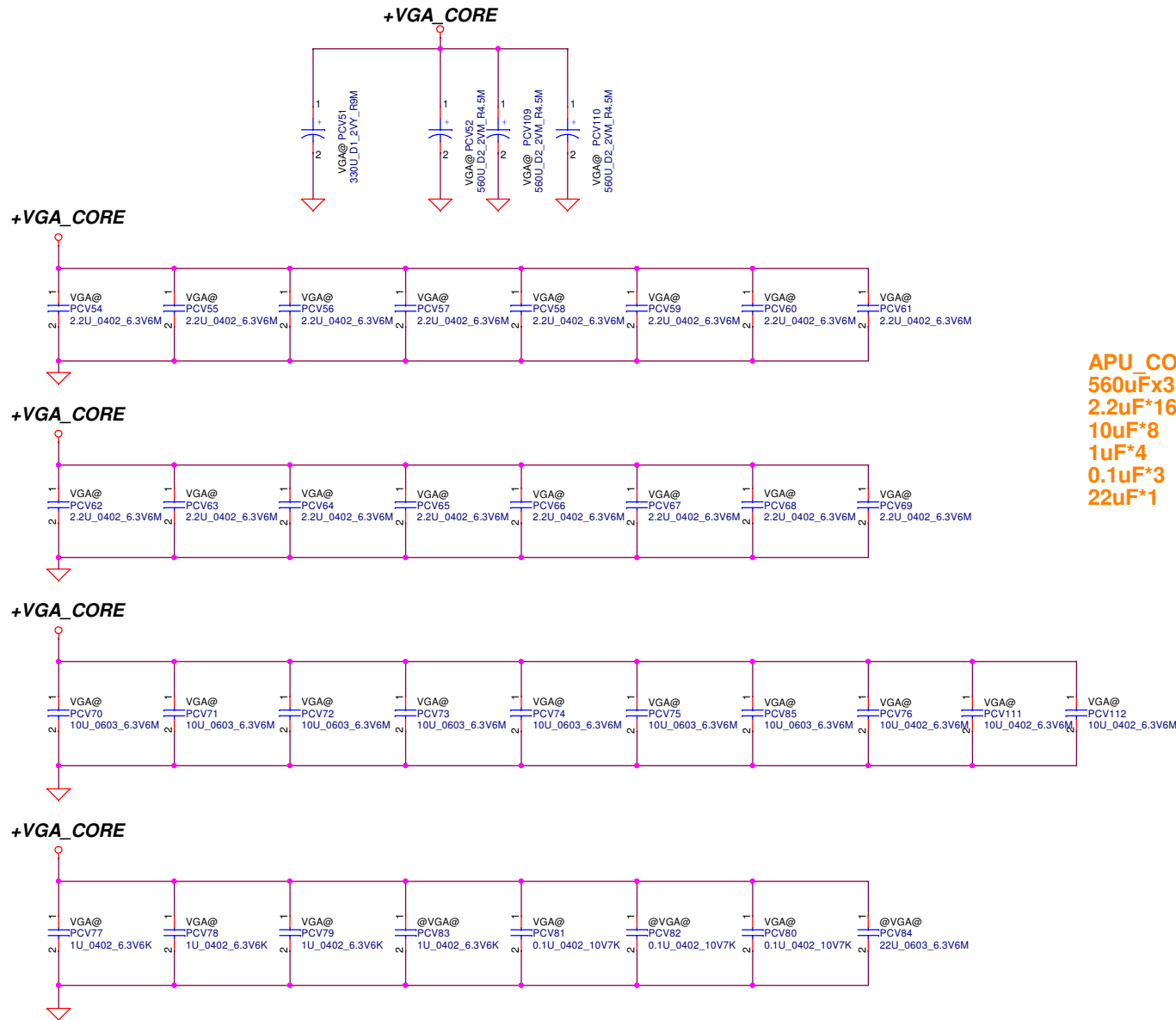






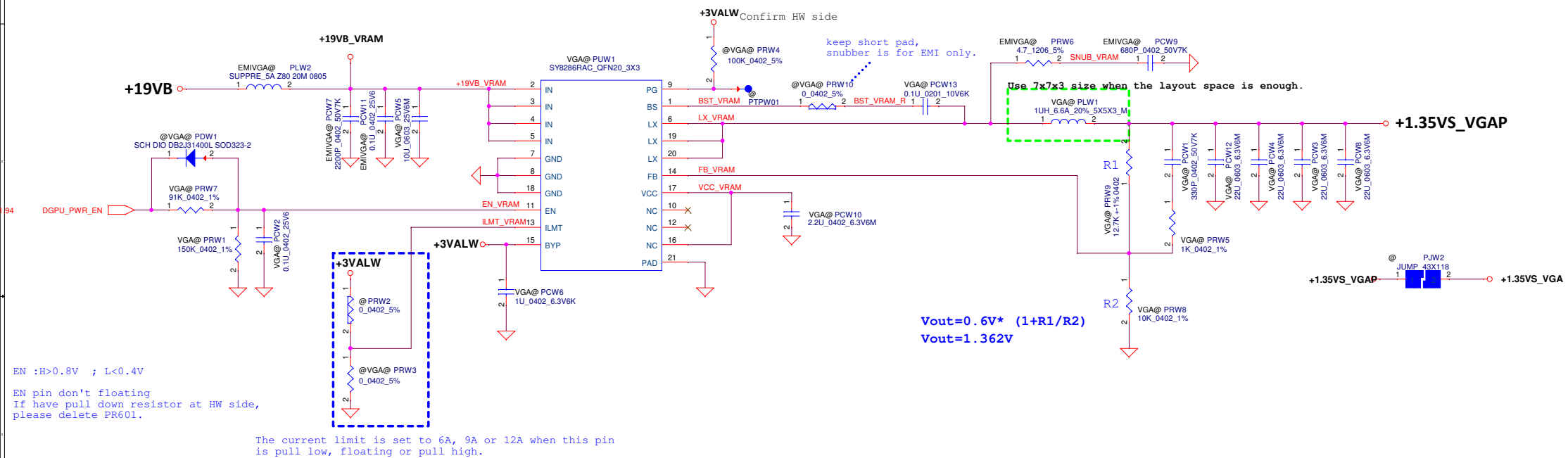
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Issued Date	2016/12/05	Deciphered Date	2017/12/05	Title	APU CORE CAP	
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					GPP53 LA-H32A	
				Date	Thursday, January 26, 2018	90 of 99





APU\_CORE\_SOC  
560uFx3+330uF  
2.2uF\*16  
10uF\*8  
1uF\*4  
0.1uF\*3  
22uF\*1

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Item	Reason for change	PG#	Modify List	Date	Phase
1	Add remote sensing to +0.8VALW	88	Add PQF1(SB000000VY00,S TR LSK3541G1ET2L 1N ) Add PRF15	12/23	PV
2	EMI Design change	82	Change PC2.PC3 from 1000P to 2200P	01/06	PV
3	APU_SOC Transient Modify	89	Add PC2134 (SGA0000AM00,S POLY C 220U 2V M D7 ESR4.5M SR H1); PCZ57.60.62.63.64.102.114.115.120 remove from BOM	01/06	PV
4	Vender change part number	85	Change from SA0000B9G00 to SA0000B9G10	01/06	PV
5	EMI Design change	89	Add PC2135 (S CER CAP 0.1U 25V K X5R 0402)	01/09	PV
6	APU_SOC Transient Modify	89	Change PRZ56 from 48.7Kohm to 75Kohm Change PC235 from 68pF to 100pF	01/09	PV
7	EMI Design change	84	Add PCB17.18.19.21.22 (S CER CAP 0.1U 25V K X5R 0402))	01/09	PV